C-ONE TECHNOLOGY CORP.

PCMCIA ATA

S-CH05 PCMCIA-ATA Card

Product Specification

Jan. 2003

Document History

Version	Description	Date	Prepared by
1	New issue	Jan. 2003	Couger Liu

Contents

1. Introduction

1.1. Introduction

This product specification reveals C-ONE Series S-CH05 PCMCIA ATA Card. It conforms to PCMCIA ATA Specification. This card provides the compatibility of read/write from PCMCIA interface into Flash Media. It can operate with 3.3V or 5V single power from the host side with high performance speed.

1.2. Related Documents and Standards

- PC Card Standard (1997), Personal Computer Memory Card International Association (PCMCIA)
- PC card ATA standard specification
  - 68 pins connector and Type II (5mm)
- Rugged stainless metal housing
- 3.3V/5V single power supply operation
- ISA standard and Read/Write is 512 byes (sector) sequential access
  - Sector Read/Write transfer rate: 8MB/sec burst
- Card density is 2GB maximum
- 3 variations of mode access
  - Memory card mode
  - I/O card mode
  - True IDE Mode
- Internal self-diagnostic program operates at Vcc power on
- High reliability based on internal ECC (Error Correcting Code) function
- Auto Sleep Function
- Data write is 300,000 cycles/block
- Operating temperature support commercial level, extended temperature and industrial level.

2. Product Specification

2.1 Operation Description

1. Operating Voltage:	Vcc Power	3.3V ± 5%;
		5V ± 5%;
2. Typical Power Consumptions:	3.3V	Read Mode: 20 mA (Max)
		Write Mode: 40 mA (Max)
		Idle Mode: <<0.3mA
	5V	Read Mode: 40 mA (Max)
		Write Mode: 60 mA (Max)
		Standby Mode: <<1mA
3. Environment conditions	Operating Temperature	0°C to 65°C
	Storage Temperature	-20°C to 85°C
	Relative Humidity	5% ~ 95%(Max.)
	Shock	50-G
	Vibration	15-G
4. System Compatibility	O/S supports DOS, Windows 98/ME/NT/2000/XP	

2.2 Physical Description

1. Weight and Measurement	Type II	L x W x H 85.6 x 54 x 5.0 (mm)
2. Storage Capacities	Capacity	32MB – 2GB
3. Performance	Data Transfer Rates	To/from Flash memory (burst mode):up to 20 Mbytes/sec
		To/from host (burst mode): up to 8 Mbytes/sec
		Sustained Read: 5 MB/sec
		Sustained Write: 2 MB/sec
		Sleep to Idle: 2 ms (max)
	Data Access Time	1.2 ms
4. Reliability	MTBF	1,000,000 hours
	Error Correction	More than 3 bit error correction per second read
	ECC	High reliability based on internal ECC function
	Endurance	100,000 Write/Erase cycles for any sector
5. Data Reliability	< 1 non-recoverable error in 10^{14} bits read	
6. Acoustic noise (at 1 m)	0 DB	

3. Product Model

3.1. Part Number Definition

P A H 0 1 G E H 6

- 6: 5: 256Mb A-mask; 6: 512Mb Mono; G: 1Gb DDP
- H: Hitachi Flash Memory Chip
- E: Controller version SAH05
- 032=32MB, 704=704MB, 01G=1GB, 1G6=1.6GB
- Hitachi Controller
- ATA Flash Card
- PCMCIA Type II

3.2. Order Information

Capacity	Part Number
32MB	PAH032EH5
64MB	PAH064EH6
96MB	PAH096EH5
128MB	PAH128EH6
160MB	PAH160EH5
256MB	PAH256EH6
320MB	PAH320EH6
512MB	PAH512EH6
704MB	PAH704EH6
1GB	PAH01GEH6
1.6GB	PAH1G6EH6
2GB	PAH02GEHG

4. Support Flash Media

4.1 Supported AND Flash Type

AND (bits)	AND Type 256Mb	AND Type 512Mb
Voltage	3.3V ± 0.3	2.7V to 3.6V

4.2 Logical Format Parameters (CHS)

Capacity:

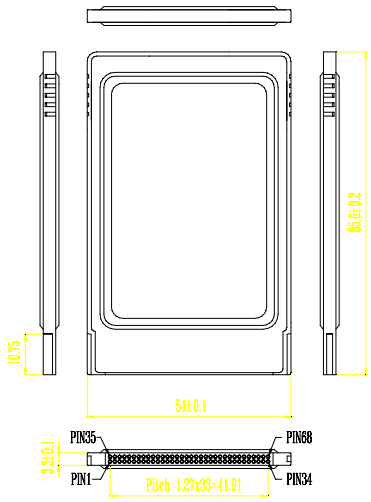
Unformatted	32M	64M	96M	128M
Cylinder	0x01E9	0x03D2	0x02DC	0x03D2
Heads	0x04	0x04	0x08	0x08
Sectors	0x20	0x20	0x20	0x20
Total Sectors	62,592	125,184	187,392	250,368

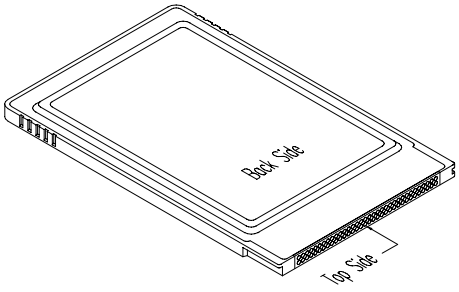
Unformatted	160M	256M	320M	512M
Cylinder	0x03D2	0x02B7	0x02E9	0x03E1
Heads	0x0A	0x0F	0x0F	0x10
Sectors	0x20	0x30	0x38	0x3F
Total Sectors	312,960	500,400	625,800	1,000,944

Unformatted	700M	1G	1.6G	2.0G
Cylinder	0x0556	0x07C3	0x0C20	0x0F86
Heads	0x10	0x10	0x10	0x10
Sectors	0x3F	0x3F	0x3F	0x3F
Total Sectors	1,376,928	2,002,896	3,128,832	4,005,792

5 Physical & Electrical Specification

5.1 PCMCIA ATA (Type II)





5.2 Electrical Specification

5.2.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Power supply	-0.3 to 5.0	V
V_{IN}	Input voltage	-0.3 to V_{CC} ± 10%	V
V_{OUT}	Output voltage	-0.3 to V_{CC} ± 10%	V
T_{STG}	Storage temperature	-40 to 85	℃
Topr	Operating temperature	0 to 70	℃

5.2.2 General DC Characteristic

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IL}	Input low current	No pull-up or pull-down	-1		1	µA
V_{IH}	Input high current	No pull-up or pull-down	-1		1	µA
V_{OZ}	Tri-state leakage current		-10		10	µA
C_{IN}	Input capacitance				15	pF
C_{OUT}	Output capacitance				15	pF

5.2.3 DC Electrical Characteristics for 5 Volts Operation

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN}	Input voltage		0		V_{CC}	V
V_{CC}	Power supply		4.5	5.0	5.5	V
T_{STG}	Storage temperature		-40		85	℃
T_{OPR}	Operating temperature		0		70	℃
V_{IL}	Input low voltage	CMOS	-0.3		$0.3\times V_{DD}$	V
V_{IH}	Input high voltage	CMOS	$0.7\times V_{DD}$		$V_{DD}+0.3$	V
V_{SIL}	Schmitt input low voltage	CMOS	1.1		2.4	V
V_{SIH}	Schmitt input high voltage	CMOS	2.8		4.0	V
V_{OL}	Output low voltage	I_{OL}=8mA			0.4	V
V_{OH}	Output high voltage	I_{OH}=-2mA	$V_{CC}-0.8$			V
R_I	Input pull-up/pull-down resister	V_{IN}=GND	10/550	45/ 110	90/50	µA/ KΩ

5.2.4 DC Electrical Characteristics for 3.3 Volts Operation

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN}	Input voltage		0		V_{CC}	V
V_{DD}	Power supply		3.0	3.3	3.6	V
T_{STG}	Storage temperature		-40		85	℃
T_{OPR}	Operating temperature		0		70	℃
V_{IL}	Input low voltage	CMOS	-0.3		$0.2\times V_{DD}$	V
V_{IH}	Input high voltage	CMOS	$0.7\times V_{DD}$		$V_{DD}+0.3$	V
V_{SIL}	Schmitt input low voltage	CMOS	1.6		2.6	V
V_{SIH}	Schmitt input high voltage	CMOS	0.7		1.7	V
V_{OL}	Output low voltage	I_{OL}=1mA			0.4	V
V_{OH}	Output high voltage	I_{OH}=-0.5mA	$V_{DD}-0.8$			V
R_I	Input pull-up/pull-down resister	V_{IN}=GND	15/230	80/ 41	230/13.7	µA/ KΩ

5.3 Power Management

5.3.1 Normal Mode

The host can reduce the power consumption of the card by changing its status with the following Power Command.

Sleep mode consumes the lowest power. Response time for the adapter to change from sleep mode to the active state is about 30 ms or less.

Standby mode, the response time is about 5ms or less. This is due to the interface of the adapter that accepts the command although can't access the media immediately

Idle mode, the adapter can respond and access the media immediately. The adapter needs longer time in this mode than in its active mode in order to active several circuits that were not used in the active mode.

Active mode, the adapter can respond and access the media immediately, and the commands are processed with no delay.

5.3.2 Power Down Mode

This adapter can set itself into Power Down mode. To enable this mode, it is needed to use the Information Change command, which is a vender unique command. The advantage of using this mode is the ability to move automatically into Sleep mode after command completion.

6 Pin Assignment

6.1 PCMCIA ATA

PC Card Memory Mode			PC Card I/O Mode			True IDE Mode		
No.	Pin Name	I/O	No.	Pin Name	I/O	No.	Pin Name	I/O
1	GND		1	GND		1	GND	
2	D03	I/O	2	D03	I/O	2	D03	I/O
3	D04	I/O	3	D04	I/O	3	D04	I/O
4	D05	I/O	4	D05	I/O	4	D05	I/O
5	D06	I/O	5	D06	I/O	5	D06	I/O
6	D07	I/O	6	D07	I/O	6	D07	I/O
7	#CE1	I	7	#CE1	I	7	#CS1	I
8	A10	I	8	A10	I	8	A10	I
9	#OE	I	9	#OE	I	9	#ATASEL	I
10	----		10	----		10	----	
11	A09	I	11	A09	I	11	A09	I
12	A08	I	12	A08	I	12	A08	I
13	----		13	----		13	----	
14	----		14	----		14	----	
15	#WE	I	15	#WE	I	15	#WE	I
16	RDY/#BSY	O	16	#IREQ	O	16	INTRQ	O
17	VCC		17	VCC		17	VCC	
18	----		18	----		18	----	
19	----		19	----		19	----	
20	----		20	----		20	----	
21	----		21	----		21	----	
22	A07	I	22	A07	I	22	A07	I
23	A06	I	23	A06	I	23	A06	I
24	A05	I	24	A05	I	24	A05	I
25	A04	I	25	A04	I	25	A04	I
26	A03	I	26	A03	I	26	A03	I
27	A02	I	27	A02	I	27	A02	I
28	A01	I	28	A01	I	28	A01	I
29	A00	I	29	A00	I	29	A00	I
30	D00	I/O	30	D00	I/O	30	D00	I/O
31	D01	I/O	31	D01	I/O	31	D01	I/O
32	D02	I/O	32	D02	I/O	32	D02	I/O
33	WP	O	33	#IOIS16	O	33	#IOIS16	O

PC Card Memory Mode			PC Card I/O Mode			True IDE Mode		
34	GND		34	GND		34	GND	
35	GND		35	GND		35	GND	
36	#CD1	O	36	#CD1	O	36	#CD1	O
37	D11	I/O	37	D11	I/O	37	D11	I/O
38	D12	I/O	38	D12	I/O	38	D12	I/O
39	D13	I/O	39	D13	I/O	39	D13	I/O
40	D14	I/O	40	D14	I/O	40	D14	I/O
41	D15	I/O	41	D15	I/O	41	D15	I/O
42	#CE2	I	42	#CE2	I	42	#CS2	I
43	#VS1	O	43	#VS1	O	43	#VS1	O
44	RESERVED		44	#IORD	I	44	#IORD	I
45	RESERVED		45	#IOWR	I	45	#IOWR	I
46	----		46	----		46	----	
47	----		47	----		47	----	
48	----		48	----		48	----	
49	----		49	----		49	----	
50	----		50	----		50	----	
51	VCC		51	VCC		51	VCC	
52	----		52	----		52	----	
53	----		53	----		53	----	
54	----		54	----		54	----	
55	----		55	----		55	----	
56	#CSEL	I	56	#CSEL	I	56	#CSEL	I
57	#VS2	O	57	#VS2	O	57	#VS2	O
58	RESET	I	58	RESET	I	58	#RESET	I
59	#WAIT	O	59	#WAIT	O	59	IORDY	O
60	RESERVED		60	#INPACK	O	60	#INPACK	O
61	#REG	I	61	#REG	I	61	#REG	I
62	BVD2	I/O	62	#SPKR	I/O	62	#DASP	I/O
63	BVD1	I/O	63	#STSCHG	I/O	63	#PDIAG	I/O
64	D08	I/O	64	D08	I/O	64	D08	I/O
65	D09	I/O	65	D09	I/O	65	D09	I/O
66	D10	I/O	66	D10	I/O	66	D10	I/O
67	#CD2	O	67	#CD2	O	67	#CD2	O
68	GND		68	GND		68	GND	

7 Signal Description

7.1 PCMCIA ATA

Signal Name	I/O	Pin	Description
A0-A10 (PC Card Memory Mode)	I	8,11,12, 22,23,24, 25,26,27, 28,29	These address lines along with the #REG signal are used to select the following: The I/O port address registers within the adapter.
A0-A10 (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
A0-A2 (True IDE Mode)		27,28,29	In True IDE Mode only A0-A2 are used to select the one of eight registers in the ATA Task File, the other address lines should be grounded.
BVD1 (PC Card Memory Mode)	I/O	63	This signal is asserted high as the BVD1 signal since a battery is not used with this adapter.
#STSCHG (PC Card I/O Mode)			This signal is asserted low to alert the host to changes in the RDY/#BSY and Write Protect states, while the I/O interface is configured. It is controlled by the Card Configure and Status Register.
#PDIAG (True IDE Mode)			In the True IDE Mode, this I/O is the Pass Diagnostic signal in the Master/Slave handshake protocol.
BVD2 (PC Card Memory Mode)	I/O	62	This signal is always driven to a high state in Memory Mode since a battery is not required for this adapter.
#SPKR (PC Card I/O Mode)			This signal is always driven to a high state in I/O Mode since this adapter does not support the audio function.
#DASP (True IDE Mode)			In the True IDE Mode, this I/O is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.
#CD1, #CD2 (PC Card Memory Mode)	O	36,67	These Card Detect pins are connected to ground on this adapter.
#CD1, #CD2 (PC Card I/O Mode)			They are used to determine if the adapter is fully inserted into the socket.

Signal Name	I/O	Pin	Description
#CD1, #CD2 (True IDE Mode)			
#CE1,#CE2 (PC Card Memory Mode)	I	7,42	These signals are used both to select the adapter and to indicate to the adapter whether a byte or a word operation is being performed. #CE2 always accesses the odd byte of the word. #CE1 accesses the even byte or the odd byte of the word depending on A0 and #CE2.
#CE1,#CE2 (PC Card I/O Mode)			
#CS1,#CS2 (True IDE Mode)			In the True IDE Mode, #CS1 is the chip select for the Task File Registers while #CS2 is used to select the Alternate Status and the Device Control Register.
#CSEL (PC Card Memory Mode)	I	56	This signal is not used for this mode.
#CSEL (PC Card I/O Mode)			This signal is not used of this mode.
#CSEL (True IDE Mode)			This internally pulled up signal is used to configure this adapter as a Master or a Slave. When this pin is grounded, this adapter is Master. When this pin is open, this adapter is Slave.
D0-D15 (PC Card Memory Mode)	I/O	41,40,39, 38,37,66, 65,64,6,5, 4,3,2,32, 31,30	These lines carry the Data, Commands and Status between the host and controller. D00 is the LSB of the even byte of the word. D08 is the LSB of the odd byte of the word.
D0-D15 (PC Card I/O Mode)			
D0-D15 (True IDE Mode)			In True IDE Mode, all Task File operations occur in the byte mode on the low order D00-D07 while all data transfers are 16 bits using D00-D15.
GND (PC Card Memory Mode)		1,34,35,68	Ground.
GND (PC Card I/O Mode)			
GND (True IDE Mode)			
RESERVED (PC Card Memory Mode)	O	60	This signal is not used in this mode.
#INPACK			The Input Acknowledge signal is asserted by

Signal Name	I/O	Pin	Description
(PC Card I/O Mode)			the adapter when the adapter is selected and responding to an I/O read cycle at the address that is on the address bus.
#INPACK (True IDE Mode)			In the True IDE mode, this signal is not used.
RESERVED (PC Card Memory Mode)	I	44	This signal is not used in this mode.
#IORD (PC Card I/O Mode)			This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the adapter when the adapter is configured to use the I/O interface.
#IORD (True IDE Mode)			In the True IDE mode, the signal is the same as the I/O Mode.
RESERVED (PC Card Memory Mode)	I	45	This signal is not used in this mode.
#IOWR (PC Card I/O Mode)			The I/O Write strobe is used to clock I/O data on the Data bus into the adapter controller registers when the adapter is configured to use the I/O interface.
#IOWR (True IDE Mode)			In the True IDE Mode, this signal is the same as the I/O mode.
#OE (PC Card Memory Mode)	I	9	This is an Output Enable Strobe generated by the host interface. It is used to read data from the adapter in Memory Mode and to read CIS and configuration registers.
#OE (PC Card I/O Mode)			In I/O Mode, this signal is used to read the CIS and configuration registers.
#ATASEL (True IDE Mode)			To enable True IDE Mode, this signal should be grounded by the host.
RDY/#BSY (PC Card Memory Mode)	O	16	In the Memory Mode, this signal is set high when adapter is ready to accept a new data transfer operation and held low when the card is busy.
#IREQ (PC Card I/O Mode)			I/O Operation. After the adapter has been configured for I/O Mode, this signal is used as Interrupt Request.
INTRQ (True IDE Mode)			In the True IDE Mode, this signal is the active high Interrupt Request to the host.

Signal Name	I/O	Pin	Description
#REG (PC Card Memory Mode)	I	61	This signal is used during Memory Cycle to distinguish between Common Memory and Attribute Memory accesses. High for Common
#REG (PC Card I/O Mode)			Memory and Low for Attribute Memory. This signal muse be low during I/O Cycles when the I/O address is on the Bus.
#REG (True IDE Mode)			In the True IDE Mode, this signal is not used and should be connected to VCC by the host.
RESET (PC Card Memory Mode) RESET (PC Card I/O Mode)	I	58	When the signal is high, the signal Resets the adapter.
#RESET (True IDE Mode)			In the True IDE Mode, the signal is the active low hardware reset from the host.
VCC (PC Card Memory Mode)		17,51	5V , 3.3V
VCC (PC Card I/O Mode)			
VCC (True IDE Mode)			
#VS1,#VS2 (PC Card Memory Mode)	O	43,57	Voltage Sense Signals.
#VS1,#VS2 (PC Card I/O Mode)			
#VS1,#VS2 (True IDE Mode)			
#WAIT (PC Card Memory Mode)	O	59	This signal is driven low by the adapter to notice the host to delay completion of the a memory of I/O cycle that is in progress.
#WAIT (PC Card I/O Mode)			
IORDY (True IDE Mode)			In the True IDE Mode, this signal may be used as IORDY.
#WE (PC Card Memory Mode)	I	15	This signal is driven by the host and used for generating memory write cycle to the registers of the adapter when the adapter is configured in the Memory mode.
#WE (PC Card I/O Mode)			In I/O mode, this signal is used for writing the configuration registers.

Signal Name	I/O	Pin	Description
#WE (True IDE Mode)			In the True IDE Mode, this signal is not used and should be connected to VCC by the host.
WP (PC Card Memory Mode)	O	33	Memory Mode, the adapter doesn't have a write protect switch. This signal is held low.
#IOIS16 (PC Card I/O Mode)			I/O Mode, A low signal indicates that a 16 bits or odd byte only operation can be performed by the addressed port.
#IOIS16 (True IDE Mode)			In the True IDE Mode, this signal is asserted low when this device is expecting a word data transfer cycle.

8. CIS and Functions Configuration Registers

8.1. Card Information Structure (CIS)

The CIS is attribute information of the card and its characteristics, which includes information about the type of card and the manufacturer. The CIS is allocated in the beginning of the attribute memory, between addresses 0 and 255. The data is allocated in the even addresses only. The Host uses these registers to initialize and configure the card.

Address	Data	7 6 5 4 3 2 1 0	Description of contents	CIS function
000H	01H	CISTPL_JEDEC	Device info tuple	Tuple code
002H	04H	TPL_LINK	Link length is 4 byte	Link to next tuple
004H	DFH	Device type W P S Device speed	Device type= DH: I/O device WPS=1:No WP Device Speed=7: ext speed	Device type, WPS, speed
006H	4AH	EXT Speed Mantissa Speed exponent	400 ns if not wait	Extended speed
008H	01H	1* 2k units	2k byte of address space	Device size
00AH	FFH	List end marker	End of device	End marker
00CH	1CH	CISTP_DEVICE_OC	Other conditions device info tuple	Tuple code
00EH	04H	TPL_LINK	Link length 4 bytes	Link to next tuple
010H	02H	EXT Reserved V_{CC} MWAIT	3V, wait is not used	Other conditions info field
012H	D9H	Device type W P S Device speed	Device type= DH: I/O device WPS=1:No WP Device Speed=1:250 ns	Device type, WPS, speed
014H	01H	1* 2k units	2k byte of address space	Device size
016H	FFH	List end marker	End of device	END marker
018H	18H	CISTPL_JEDEC_C	JEDEC ID common memory	Tuple code
01AH	02H	TPL_LINK	Link length is 2 bytes	Link to next tuple
01CH	DFH	PCMCIA's manufacturer's JEDEC ID Code	Manufacturer's ID code	JEDEC ID of PC Card ATA
01EH	01H	PCMCIA JEDEC device code	2nd byte of JEDEC ID	
020H	20H	CISTPL_MANFID	Manufacturer's ID code	Tuple code
022H	04H	TPL_LINK	Link length is 4 bytes	Link to next tuple
024H	07H	Low byte of PCMCIA manufacturer's code	HITACHI JEDEC manufacturer's ID	Low byte of manufacturer's ID code
026H	00H	High byte of PCMCIA manufacturer's code	Code of 0 because other byte is JEDEC 1 byte manufacturer's ID	High byte of manufacturer's ID code

028H	00H	Low byte of product code	HITACHI code for PC CARD ATA	Low byte of product code
02AH	00H	High byte of product code		High byte of product code

Address	Data	7 6 5 4 3 2 1 0	Description of contents	CIS function
02CH	15H	CISTPL_VERS_1	Level 1 version/product info	Tuple code
02EH	15H	TPL_LINK	Link length is 15 bytes	Link to next tuple
030H	04H	TPPLV1_MAJOR	PCMCIA2.0/JEIDA4.1	Major version
032H	01H	TPPLV1_MINOR	PCMCIA2.0/JEIDA4.1	Minor version
034H	48H		'H'	Info string 1
036H	49H		'I'	
038H	54H		'T'	
03AH	41H		'A'	
03CH	43H		'C'	
03EH	48H		'H'	
040H	49H		'I'	
042H	00H		Null terminator	
044H	46H		'F'	Info string 2
046H	4CH		'L'	
048H	41H		'A'	
04AH	53H		'S'	
04CH	48H		'H'	
04EH	00H		Null terminator	
050H	35H		'5'	Vender specific strings
052H	2EH		'.'	
054H	30H		'0'	
056H	00H		Null terminator	
058H	FFH	List end marker	End of device	END marker
05AH	21H	CISTPL_FUNCID	Function ID tuple	Tuple code
05CH	02H	TPL_LINK	Link length is 2 bytes	Link to next tuple
05EH	04H	TPLFID_FUNCTION=04H	Disk function, may be silicon, may be removable	PC card function code
060H	01H	Reserved R P	R=0: No BIOS ROM P=1: Configure card at power on	System initialization byte

Address	Data	7 6 5 4 3 2 1 0	Description of contents	CIS function
062H	22H	CISTPL_FUNCE	Function extension tuple	Tuple code
064H	02H	TPL_LINK	Link length 2 bytes	Link to next tuple
066H	01H	Disk function extension tuple type	Disk interface type	Extension tuple type for disk
068H	01H	Disk interface type	PC card AtA interface	Interface type
06AH	22H	CISTPL_FUNCE	Function extension tuple	Tuple code
06CH	03H	TPL_LINK	Link length is 3 bytes	Link to next tuple
06EH	02H	Disk function extension tuple type	Single drive	Extension tuple type for disk
070H	0CH	Reserve D U S V	No V_{pp}< Silicon, single drive V=0: No V_{pp} required S=1: Silicon U=1: Unique serial# D=0: Single drive on card	Basic ATA option Parameter byte 2
072H	0FH	R I E N P3 P2 P1 P0	P0: Sleep mode supported P1: Standby mode supported P2: Idle mode supported P3: Drive auto power control N: Some config excludes 3X7 E: Index bit is emulated I: Twin IOIS 16# datd reg only R: Reserved	Basic ATA option parameter byte 2
074H	1AH	CISTPL_CONFIG	Configuration tuple	Tuple code
076H	05H	TPL_LINK	Link length is 5 bytes	Link to next tuple
078H	01H	RFS RMS RAS	RFS: Reserved RMS: TPCC_RMSK size-1=0 RAS:TPCC_RADR size-1=1 l byte register mask 2 byte config base address	Size of fields byte TPCC_SZ
07AH	03H	TPCC_LAST	Entry with config index of 03H is final entry in table	Last entry of config registers
07CH	00H	TPCC_RADR(LSB)	Configuration registers are located at 200H in REG space	Location of config registers
07EH	02H	TPCC_RADAR(MSB)		
080H	0FH	Reserved S P C I	I: Configuration index C: configuration and status P: Pin replacement S: Socket and copy	Configuration registers present mask TPCC_RMSK

Address	Data	7 6 5 4 3 2 1 0	Description of contents	CIS function
082H	1BH	CISTPL_CFTABLE_ENTRY	Configuration table entry tuple	Tuple code
084H	08H	TPL_LINK	Link length is 8 bytes	Link to next tuple
086H	C0H	I D Configuration Index	Memory mapped I/O configuration I=1: Interface byte follows D=1: Default entry Configuration index=0	Configuration table index byte TPCE_INDX
088H	40H	W R P B Interface type	W=0: Wait not used R=1: Ready active P=0: WP not used B=0: BVD1and BVD2 not used IF type=0: Memory interface	Interface description field TPCE_IF
08AH	A1H	M MS IR IO T P	M=1: Misc info present MS=01: Memory space info single 2-byte length IR=0: No interrupt info present IO=0: No I/O port info present T=0: No toming info present P=1: V_{cc} only info	Feature selection TPCE_FS
08CH	01H	R DI PI AI SI HV LV NV	Nominal voltage only follows R: Reserved DI: Power down current info PI: Peak current info AI: Average current info SI: Static current info HV: Max voltage info LV: Min voltage info NV: Nominal voltage info	Power parameters for V_{cc}
08EH	55H	X Mantissa Exponent	Nominal voltage=5V	V_{cc} nominal value
090H	08H	Length in 256 bytes pages (LSB)	Length of memory space is 2 kB	Memory space description structures (TPCE_MS)
092H	00H	Length in 256 bytes pages (MSB)		
094H	20H	X R P RO A T	X=0: No more misc fields R: Reserved P=1: Power down supported RO=0: Not read only mode A=0: Audio not supported T=0: Single drive	Miscellaneous features field TPCE_MI

Address	Data	7 6 5 4 3 2 1 0	Description of contents	CIS function
096H	1BH	CISTPL_CFTABLE_ENTRY	Configuration table entry tuple	Tuple code
098H	06H	TPL_LINK	Link length is 6 bytes	Link to next tuple
09AH	00H	I D Configuration Index	Memory mapped I/O configuration I=0: No interface byte D=0: No Default entry Configuration index=0	Configuration table index TPCE_INDX
09CH	01H	M MS IR IO T P	M=0: No misc info MS=00: No memory space inflo IO=0: No I/O port info present T=0:No timing info present P=0: V_{cc} only info	Feature selection byte TPCE_FS
09EH	21H	R DI PI AI SI HV LV NV	Nominal voltage only follows R: Reserved DI: Power down current info PI: Peak current info AI: Average current info SI: Static current info HV: Max voltage info LV: Min voltage info NV: Nominal voltage info	Power parameters for V_{cc}
0A0H	B5H	X Mantissa Exponent	Nominal Voltage=3.0V	V_{cc} nominal value
0A2H	1EH	X Extension	+0.3 V	Extension byte
0A4H	4DH	X Mantissa Exponent	Max average current over 10 msec is 45 mA	Max. average current

Address	Data	7 6 5 4 3 2 1 0	Description of contents	CIS function
0A6H	1BH	CISTPL_CFTABLE_ENTRY	Configuration table entry tuple	Tuple code
0A8H	C1H	TPL_LINK	Link length is 10 bytes	Link to next tuple
0AAH	C1H	I D Configuration INDEX	Contiguous I/O mapped ATA registers configuration I=1: Interface byte follows D=1: Default entry Configuration index=1	Configuration table index byte TPCE_INDX
0ACH	41H	W R P B Interface type	W=0: Wait not used R=1: Ready active P=0: WP not used B=0: BVS1 and BVS2 not used IF type=1: I/O interface	Interface description field TPCE_IF
0AEH	99H	M MS IR IO T P	M=1: Misc info present MS=00: No memory space info IR=1: Interrupt info present IO=1: I/O port info present T=0: No timing info present P=1:Vcc only info	Feature selection byte TPCE_FS
0B0H	01H	R DI PI AI SI HV LV NV	Nominal voltage only follows R: Reserved DI: Power down current info PI: Peak current info AI: Average current info SI: Static current info HV: Max voltage info LV: Min voltage info NV: Nominal voltage info	Power parameters for Vcc
0B2H	55H	X Mantissa Exponent	Nominal Voltage=5V	Vcc nominal value
0B4H	64H	R S E IO AddrLine	S=1: 16-bit hosts supported E=1: 8-bit hosts supported IO AddrLine:4 lines decoded	I/O space description field TPCE_IO
0B6H	F0H	S P L M V B I N	S=1: Share logic active P=1: Pulse mode IRQ supported L=1: Level mode IRQ supported M=1: Bit mask of IRQ present V=0: No vender unique IRQ B=0: No bus error IRQ I=0: No IO check IRQ N=0: No NMI	Interrupt request description structure TPCE_IR

Address	Data	7	6	5	4	3	2	1	0	Description of contents	CIS function
0B8H	FFH	IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	ORQ2	IRQ1	0	IRQ level to be routed 0 to 15 recommended	Mask extension byte 1 TPCE_IR
0BAH	FFH	IRQ15	IRQ14	IRQ13	IRQ12	IRQ11	ORQ10	IRQ9	8	Recommended routing to any “normal, maskable” IRQ	Mask extension byte 2 TPCE_IR
0BCH	20H	X	R	P	R	O	A	T		X=0: Nomore misc fields R: reserved P=1: Power down supported RO=0: Not read only mode A=0: Audi not supported T=0: Single drive	Miscellaneous features field TPCE_MI

Address	Data	7 6 5 4 3 2 1 0	Description of contents	CIS function
0BEH	1BH	CISTPL_CFTABLE_ENTRY	Configuration table entry tuple	Tuple code
0C0H	06H	TPL_LINK	Link length is 6 bytes	Link to next tuple
0C2H	01H	I D Configuration index	Contiguous I/O mapped ATA registers configuration I=0: No Interface byte D=0: No Default entry Configuration index=1	Configuration table index byte TPCE_INDX
0C4H	01H	M MS IR IO T P	M=0: No Misc info present MS=00: No memory space info IR=0: No Interrupt info present IO=0: No I/O port info present T=0: No timing info present P=1:Vcc only info	Feature selection byte TPCE_FS
0C6H	21H	R DI PI AI SI HV LV NV	Nominal voltage only follows R: Reserved DI: Power down current info PI: Peak current info AI: Average current info SI: Static current info HV: Max voltage info LV: Min voltage info NV: Nominal voltage info	Power parameters for Vcc
0C8H	B5H	X Mantissa Exponent	Nominal voltage =3.0V	Vcc nominal value
0CAH	1EH	X Extension	+0.3V	Extension byte
0CCH	4DH	X Mantissa Exponent	Max average current over 10 msec is 45mA	Max. average current

Address	Data	7 6 5 4 3 2 1 0	Description of contents	CIS function
0CEH	1BH	CISTPL_CFTABLE_ENTRY	Configuration table entry tuple	Tuple code
0D0H	0FH	TPL_LINK	Link length is 15 bytes	Link to next tuple
0D2H	C2H	I D Configuration index	Contiguous I/O mapped ATA registers configuration I=1: Interface byte follows D=1: Default entry follows Configuration index=2	Configuration table index byte TPCE_INDX
0D4H	41H	W R P B Interface type	W=0: Wait not used R=1: Ready active P=0: WP not used B=0: BVS1 and BVS2 not used IF type=1: I/O interface	Interface description field TPCE_IF
0D6H	99H	M MS IR IO T P	M=1: Misc info present MS=00: No memory space info IR=1: Interrupt info present IO=1: I/O port info present T=0: No timing info present P=1:V_{cc} only info	Feature selection byte TPCE_FS
0D8H	01H	R DI PI AI SI HV LV NV	Nominal voltage only follows R: Reserved DI: Power down current info PI: Peak current info AI: Average current info SI: Static current info HV: Max voltage info LV: Min voltage info NV: Nominal voltage info	Power parameters for V_{cc}
0DAH	55H	X Mantissa Exponent	Nominal Voltage=5V	V_{cc} nominal value
0DCH	EAH	R S E IO AddrLine	R=1: Range follows S=1:16-bit hosts supported E=1: 8-bit hosts supported IO AddrLines: 10 lines decoded	I/O space description field TPCE_IO

Address	Data	7	6	5	4	3	2	1	0	Description of contents	CIS function
0E0H	FOH									1st I/O base address(LSB)	1st I/O range address
0E2H	01H									1st I/O base address(MSB)	
0E4H	07H									1st I/O length-1	1st I/O range length
0E6H	F6H									2nd I/O base address(LSB)	2nd I/O range address
0E8H	03H									2nd I/O base address(MSB)	
0EAH	01H									2nd I/O length-1	2nd I/O range length
0ECH	EEH	S	P	L	M	IRQ level				S=1: Share logic active P=1: Pulse mode IRQ supported L=1: Level mode IRQ supported M=0: Bit mask of IRQ present IRQ level is ORQ 14	Interrupt request description structure TPCE_IR
0EEH	20H	X	R	P	R	O	A		T	X=0: Nomore misc fields R: reserved P=1: Power down supported RO=0: Not read only mode A=0: Audi not supported T=0: Single drive	Miscellaneous features field TPCE_MI

Address	Data	7 6 5 4 3 2 1 0	Description of contents	CIS function
0F0H	1BH	CISTPL_CFTABLE_ENTRY	Configuration table entry tuple	Tuple code
0F2H	06H	TPL_LINK	Link length is 15 bytes	Link to next tuple
0F4H	02H	I D Configuration index	ATA primary I/O mapped configuration I=0: No Interface byte D=0: No Default entry Configuration index=2	Configuration table index byte TPCE_INDX
0F6H	01H	M MS IR IO T P	M=0: No Misc info MS=00: No memory space info IR=0: No Interrupt info present IO=0: No I/O port info present T=0: No timing info present P=1: Vcc only info	Feature selection byte TPCE_FS
0F8H	21H	R DI PI AI SI HV LV NV	Nominal voltage only follows R: Reserved DI: Power down current info PI: Peak current info AI: Average current info SI: Static current info HV: Max voltage info LV: Min voltage info NV: Nominal voltage info	Power parameters for Vcc
0FAH	B5H	X Mantissa Exponent	Nominal voltage =3.0V	Vcc nominal value
0FCH	1EH	X Extension	+0.3V	Extension byte
0FEH	ADH	X Mantissa Exponent	Max average current over 10 msec is 45mA	Max. average current

Address	Data	7 6 5 4 3 2 1 0	Description of contents	CIS function
100H	1BH	CISTPL_CFTABLE_ENTRY	Configuration table entry tuple	Tuple code
102H	0FH	TPL_LINK	Link length is 15 bytes	Link to next tuple
104H	C3H	I D Configuration index	ATA secondary I/O mapped configuration I=1: Interface byte follow D=1: Default entry Configuration index=3	Configuration table index byte TPCE_INDX
106H	41H	W R P B Interface type	W=0: Wait not used R=1: Ready active P=0: WP not used B=0: BVS1 and BVS2 not used IF type=1: I/O interface	Interface description field TPCE_IF
108H	99H	M MS IR IO T P	M=1: Misc info present MS=00: No memory space info IR=1: Interrupt info present IO=1: I/O port info present T=0: No timing info present P=1:Vcc only info	Feature selection byte TPCE_FS
10AH	01H	R DI PI AI SI HV LV NV	Nominal voltage only follows R: Reserved DI: Power down current info PI: Peak current info AI: Average current info SI: Static current info HV: Max voltage info LV: Min voltage info NV: Nominal voltage info	Power parameters for Vcc
10CH	55H	X Mantissa Exponent	Nominal Voltage=5V	Vcc nominal value
10EH	EAH	R S E IO AddrLine	R=1: Range follows S=1:16-bit hosts supported E=1: 8-bit hosts supported IO AddrLines: 10 lines decoded	I/O space description field TPCE_IO
110H	61H	LS AS N range	LS=1: Size of lengths is 1 byte AS=2: Size of address is 2 bytes N Range=1: Address range-1	I/O range format description

Addres	Data	7 6 5 4 3 2 1 0	Description of contents	CIS function
112H	70H		1st I/O base address(LSB)	1st I/O range address
114H	01H		1st I/O base address(MSB)	
116H	07H		1st I/O length-1	1st I/O range length
118H	76H		2nd I/O base address(LSB)	2nd I/O range address
11AH	03H		2nd I/O base address(MSB)	
11CH	01H		2nd I/O length-1	2nd I/O range length
11EH	EEH	S P L M IRQ level	S=1: Share logic active P=1: Pulse mode IRQ supported L=1: Level mode IRQ supported M=0: Bit mask of IRQ present IRQ level is ORQ 14	Interrupt request description structure TPCE_IR
120H	20H	X R P RO A T	X=0: Nomore misc fields R: reserved P=1: Power down supported RO=0: Not read only mode A=0: Audi not supported T=0: Single drive	Miscellaneous features field TPCE_MI

Address	Data	7 6 5 4 3 2 1 0	Description of contents	CIS function
122H	1BH	CISTPL_CFTABLE_ENTRY	Configuration table entry tuple	Tuple code
124H	06H	TPL_LINK	Link length is 6 bytes	Link to next tuple
126H	03H	I D Configuration index	ATA secondary I/O mapped configuration I=0: No Interface byte D=0: No Default entry Configuration index=3	Configuration table index byte TPCE_INDX
128H	01H	M M S I R I O T P	M=0: No Misc info MS=00: No memory space info IR=0: No Interrupt info present IO=0: No I/O port info present T=0: No timing info present P=1: V_{cc} only info	Feature selection byte TPCE_FS
12AH	21H	R DI PI AI SI HV LV NV	Nominal voltage only follows R: Reserved DI: Power down current info PI: Peak current info AI: Average current info SI: Static current info HV: Max voltage info LV: Min voltage info NV: Nominal voltage info	Power parameters for V_{cc}
12CH	B5H	X Mantissa Exponent	Nominal voltage =3.0V	V_{cc} nominal value
12EH	1EH	X Extension	+0.3V	Extension byte
130H	4DH	X Mantissa Exponent	Max average current over 10 msec is 45mA	Max. average current
132H	14H	CISTPL_NO_LINK	No link control tuple	Tuple code
134H	00H		Link is 0 bytes	Link to next tuple
136H	FFH	CISTPL_END	End of tuple	Tuple code

8.2 Configuration Option Register (200H)

This register is used for the configuration of the card and allows issuing software reset through this register.

<Read/Write, Reset value = 001H>

D7	D6	D5	D4	D3	D2	D1	D0
SRESET	LevlREQ	INDEX					
R/W	R/W	R/W					

Index Those bits are used for selecting an operation mode of the card as follows. When Power on, Card Hard Reset and Soft Rest, this data is “000000” for the Memory mode card interface recognition.

LevlREQ This bit sets to “0” when pulse mode interrupt is selected, and “1” when level mode interrupt is selected.

SRESET Setting this bit to “1”, places the card in the reset state (Card Hard Reset).This operation is equal to Hard Reset, except this bit is not cleared. Card configuration status is reset and the card internal initialized operation starts when Card Hard Reset is executed, so next access to the card should be the same sequence as the power on sequence.

Index Bits Assignment

INDEX bits						Task File register address	Mapping mode
5	4	3	2	1	0		
0	0	0	0	0	0	OH to FH, 400h to 7FFH	Memory mode
0	0	0	0	0	1	xx0H to xxFH	Independent I/O mode
0	0	0	0	1	0	1F0H to 1F7H, 3F6H to 3F7H	Primary I/O mapped
0	0	0	0	1	1	170H to 177H, 376H to 377H	Secondary I/O mapped

8.3 Card Configuration And Status Register (Address 202H)

This register is used for observing the card state.

<Read/Write, Reset value = 001H>

D7	D6	D5	D4	D3	D2	D1	D0
CHGED	SIGCHG	IOIS8	0	0	PWD	INTR	0
0/R	0/R	R/W	---	---	R/W	R	---

INTR INTERRUPT: When set, indicates that the #IREQ pin is low. When clear, indicates that the #IREQ pin is high. This bit state is available whether I/O card interface has been configured or not. If interrupts are disabled by the #IEN bit in the Device Control Register, this bit is zero.

PWD POWER DOWN: When set, the card enters sleep state (Power Down mode). When clear, the card transfers to idle state (active mode).

IOIS8 I/O IS 8 bit: When set, indicates that the data bus width of the host is 8 bits (D0-D7). When clear, indicates that the data bus width of the host is 16 bits (D0-D15).

SIGCHG SIGNAL CHGED: This bit is set and reset by the host to enable and disable a state-change signal from the Status Register, the CHANGED bit control pin 46 and the CHANGED Status signal. If no state change signal is desired, this bit should be set to zero (0) and pin 46 (#STSCHG) signal will be held high while thie card is configured for I/O.

CHGED Indicated that one or both of the pin Replacement Register (204H) Crdy, or CWProt bits are set to one (1). When changed bit is set, #STSCHG pin 46 is held low if the SIGCHG bit is a one (1) and the card is configured for I/O interface.

8.4 Pin Replacement Register (Address 204H)

This register is used for providing the signal state of #IREQ signal when the card configured I/O card interface.

<Read, Reset value = 0CH>

D7	D6	D5	D4	D3	D2	D1	D0
0	0	CRDY	CWProt	RBVD1	RBVD2	RRDY	RWProt
---		RW		1		1/R	R/R/W

RWProt READ WRITE PROTECT: this bit indicates the write protect status. When set, indicates write protect. When cleared indicates write is enable.

PRDY This bit is used to determine the internal state of the RDY/BSY signal. This bit may be used to determine the state of the Ready/Busy as this pin has been reallocated for use as interrupt Request on an I/O card.

CEProt This bit is set to one (1) when RWProt changes state. This bit may be written by

the host.

CRDY CARD READY: This bit is set to one (1) when the READY bit changes state. This bit may be written by the host.

8.5 Socket and Copy Register (Address 206H)

This register is used for identification of the card from other cards. The host can read and write this register. The host shall set this register before the card's Configuration Option Register is set.

<Read, Reset value = 00H>

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	DRV#	0	0	0	0
---	---	---	R/W	---	---	---	---

DRV# DRIVE NUMBER: This bit is set by the host and compared to the DRV bit (D4), in the ATA Drive/Head Register.

9. ATA Specific Register Definitions

As we described the adapter provides several kinds of addressing modes, Memory mode, I/O mode, and True IDE. Below are described the procedures access for accessing each mode the Task File registers.

9.1 Memory Mapped Addressing

Memory Mapped Addressing

#REG	Offset	A10	A4 – A9	A3	A2	A1	A0	#OE = "0"	#WE = "0"
1	0H	0	X	0	0	0	0	Even read data	Even write data
1	1H	0	X	0	0	0	1	Error	Feature
1	2H	0	X	0	0	1	0	Sector Count	Sector Count
1	3H	0	X	0	0	1	1	Sector Number	Sector Number
1	4H	0	X	0	1	0	0	Cylinder Low	Cylinder Low
1	5H	0	X	0	1	0	1	Cylinder High	Cylinder High
1	6H	0	X	0	1	1	0	Drive/Head	Drive/Head
1	7H	0	X	0	1	1	1	Status	Command
1	8H	0	X	1	0	0	0	Duplicate Even Read Data	Duplicate Even Write Data
1	9H	0	X	1	0	0	1	Duplicate Odd Read Data	Duplicate Odd Write Data
1	DH	0	X	1	1	0	1	Duplicate Error	Duplicate Feature
1	EH	0	X	1	1	1	0	Alternate Status	Device Control
1	FH	0	X	1	1	1	1	Drive Address	Reserved
1	8H	1	X	X	X	X	0	Even Read Data	Even Write Data
1	9H	1	X	X	X	X	1	Odd Read Data	Odd Write Data

9.2 Contiguous I/O Mapping Addressing

Contiguous I/O Mapping Addressing

#REG	Offset	A10	A4 – A9	A3	A2	A1	A0	#IORD = "0"	#IOWR = "0"
0	0H	0	X	0	0	0	0	Even read data	Even write data
0	1H	0	X	0	0	0	1	Error	Feature
0	2H	0	X	0	0	1	0	Sector Count	Sector Count
0	3H	0	X	0	0	1	1	Sector Number	Sector Number
0	4H	0	X	0	1	0	0	Cylinder Low	Cylinder Low
0	5H	0	X	0	1	0	1	Cylinder High	Cylinder High
0	6H	0	X	0	1	1	0	Drive/Head	Drive/Head
0	7H	0	X	0	1	1	1	Status	Command
0	8H	0	X	1	0	0	0	Duplicate Even Read Data	Duplicate Even Write Data
0	9H	0	X	1	0	0	1	Duplicate Odd Read Data	Duplicate Odd Write Data
0	DH	0	X	1	1	0	1	Duplicate Error	Duplicate Feature
0	EH	0	X	1	1	1	0	Alternate Status	Device Control
0	FH	0	X	1	1	1	1	Drive Address	Reserved

9.3 Overlapping I/O Mapping Addressing

Overlapping I/O Mapping (Primary, Secondary) Addressing

#REG	A10	A4 – A9		A3	A2	A1	A0	#IORD= "0"	#IOWR ="0"
		Primary	Secondary						
0	X	1FH	17H	0	0	0	0	Even read data	Even write data
0	X	1FH	17H	0	0	0	1	Error	Feature
0	X	1FH	17H	0	0	1	0	Sector Count	Sector Count
0	X	1FH	17H	0	0	1	1	Sector Number	Sector Number
0	X	1FH	17H	0	1	0	0	Cylinder Low	Cylinder Low
0	X	1FH	17H	0	1	0	1	Cylinder High	Cylinder High
0	X	1FH	17H	0	1	1	0	Drive/Head	Drive/Head
0	X	1FH	17H	0	1	1	1	Status	Command
0	X	3FH	37H	1	1	1	0	Alternate Status	Device Control
0	X	3FH	37H	1	1	1	1	Drive Address	Reserved

9.4 True IDE Mode

True IDE Mode

#CS0	#CS1	DA2	DA1	DA0	#IORD = "0"	#IOWR = "0"
1	1	X	X	X	Hi-Z	Not Used
1	0	0	X	X	Hi-Z	Not Used
1	0	1	0	X	Hi-Z	Not Used
0	0	X	X	X	Invalid	Invalid
1	0	1	1	0	Alternate Status	Device Control
1	0	1	1	1	Device Address	Not Used
0	1	0	0	0	Data	Data
0	1	0	0	1	Error	Feature
0	1	0	1	0	Sector Count	Sector Count
0	1	0	1	1	Sector Number	Sector Number
0	1	1	0	0	Cylinder Low	Cylinder Low
0	1	1	0	1	Cylinder High	Cylinder High
0	1	1	1	0	Drive/Head	Drive/Head
0	1	1	1	1	Status	Command

9.5 ATA Registers

9.5.1. Data Register

The Data register is a 16-bit register used to transfer data blocks between the ATA data buffer and the host. In addition, the Format Track command uses this register to transfer the sector-information. Setting this mode requires calling the Set Features command.

bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
D7	D6	D5	D4	D3	D2	D1	D0

bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8
D15	D14	D13	D12	D11	D10	D9	D8

9.5.2. Error Register

The Error Register contains additional information about the source of an error. The information in the register is only valid when an error is indicated in ERR-bit (bit-0 = 1) of the Status Register.

bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
BBK	UNC	MC	IDNF	MCR	ABRT	T0NF	AMNF

BBK	Bad Block mark detected in the requested sector ID field - Not supported
UNC	Non-Correctable data error encountered
MC	Removable media access ability has changed - not supported (is 0)
IDNF	Requested sector ID-field Not Found
MCR	Media Change Request indicates that the removable-media drive's latch has changed, indicating that the user wishes to remove the media - not supported (is 0)
ABRT	Drive status error or Aborted invalid command
T0NF	Track 0 Not Found during a *Recalibrate* command - Not supported
AMNF	Address Mark Not Found after finding the correct ID field - Not supported

9.5.3. Feature Register

This register enables drive-specific features. See the Set Features or Get/Set Features command descriptions.

bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
Feature byte							

9.5.4. Sector Count Register

The Sector Count Register contains the number of data sectors requested to be transferred during a read or write operation between the host and the adapter. A zero register value specifies 256 sectors. The command was successful if this register is zero at command completion. If the request is not completed, the register contains the number of sectors left to be transferred.

Some commands (e.g. Initialize Drive Parameters or Format Track) may redefine the register's contents.

bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
Sector count byte							

9.5.5. Sector Number Register

In the CHS (Cylinder, Head, Sector) mode, the Sector Number register contains the subsequent command's starting sector number, which can be from 1 to the maximum number of sectors per track. In LBA (logical block address) mode, this register contains LBA bits 0-7, which are updated at command completion. See the command descriptions for register contents at command completion (whether successful or unsuccessful).

bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
SN7	SN6	SN5	SN4	SN3	SN2	SN1	SN0
LBA7	LBA6	LBA5	LBA4	LBA3	LBA2	LBA1	LBA0

SN0 – SN7 Sector number byte (8-bits)
LBA0 – LBA7 LBA bits 0 to 7

9.5.6. Cylinder Low Register

In the CHS mode, the Cylinder Low Register contains the cylinder number low-8 bits and reflects their status at command completion. In LBA mode, this register contains LBA bits 8-15 and reflects their status at command completion.

bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
CL7	CL6	CL5	CL4	CL3	CL2	CL1	CL0
LBA15	LBA14	LBA13	LBA12	LBA11	LBA10	LBA9	LBA8

CL0 – CL7	Cylinder Low byte (8-bits)
LBA8 – LBA15	LBA bits 8 to 15

9.5.7. Cylinder High Register

In the CHS mode, the Cylinder High Register contains the cylinder numbers high-8 bits and reflects their status at command completion. In LBA mode, this register contains LBA bits 16-23 and reflects their status at command completion.

bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
LBA23	LBA22	LBA21	LBA20	LBA19	LBA18	LBA17	LBA16

CH0 – CH7	Cylinder High byte (8-bits)
LBA16 – LBA23	LBA bits 16 to 23

9.5.8. Drive Head Register

The Drive/Head Register is used to select the drive and head (heads minus 1, when executing *Initialize Drive Parameters* command). It is also used to select the LBA addressing instead of the CHS addressing.

bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
1	LBA	1	DRV	HS3 / LBA27	HS2 / LBA26	HS1 / LBA25	HS0 / LBA24

HS0-HS3/	Head number.
DRV	Drive select number. When DRV=0, the master drive is selected. When DRV=1, the Slave drive is selected.
LBA24-LBA27	MSB of the LBA addressing.
LBA	Address mode select. 0 = CHS (Cylinder, Head, Sector) mode. 1 = LBA (Logical Block Address) mode.

9.5.9. Status Register

This register contains the adapter status. The contents of this register are updated to reflect the current state of the adapter and the progress of any command being executed by the adapter. When the BSY bit is equal to zero, the other bits in this register are valid. When the BSY bit is equal to one, the other bits in this register are not valid. When the register is read, the interrupt (#IREQ pin) is cleared.

bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
BSY	DRDY	DWF	DSC	DRQ	CORR	0	ERR

ERR	When set, indicates that an error has occurred during the previous command execution. The bits in the Error Register indicate the cause.
IDX	Index is not used – always set to Zero.
CORR	Indicates that a data error was corrected; transfer is not terminated.
DRQ	Data Request. When set, indicates that the adapter is ready to transfer a word or byte of data between the host and the adapter.
DSC	Drive Seek Complete. When set, indicates that the requested sector was found.
DWF	Drive Write Fault status. When set, indicates that an error has occurred during write.
DRDY	Indicates whether the adapter is capable of performing drive operations (commands). This bit is cleared at power up and remains cleared until the drive is ready to accept a command. On error, DRDY changes only after the host reads the Status register.
BSY	This signal is set during the time the adapter accesses the command buffer or the registers. During this time the host is locked out from accessing the command register and buffer. As long as this bit is set no bits in the register are valid.

9.5.10. Alternate Status Register

The Alternate Status Register contains command block status information (see Status register). Unlike the Status register, reading this register does not acknowledge or clear an interrupt.

bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
BSY	DRDY	DWF	DSC	DRQ	CORR	0	ERR

9.5.11. Device Control Register

The Device Control Register is used to control the drive interrupt request and issue an ATA soft reset to the drive.

bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
---	---	---	---	---	SRST	#IEN	0

#IEN	INTERRUPT ENABLE: When set (0), it enables interrupts to the host (using the #IREQ tri-state pin). When inactive (1) or drive is not selected, it disables all pending interrupts (#IREQ in high-Z). This bit is ignored in Memory mode.
SRST	SOFT RESET: When set, forces the ATA to perform an AT disk control soft reset operation.

9.5.12. Drive Address Register

This register reflects the drive and its heads.

bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
High-Z	#WTG	#HS3	#HS2	#HS1	#HS0	#DS1	#DS0

#DS0	When set (0), it indicates that drive 0 is active and selected.
#DS1	When set (0), it indicates that drive 1 is active and selected.
#HS0 - #HS3	Negation of the head number in the Drive/Head Register.
#WTG	When set (0), it indicates that a write operation is in progress, otherwise it is inactive (1) - not supported.

Note: Addressing Mode Descriptions - The adapter, on a command by command basis, can operate in either CHS or LBA addressing modes. Identify Drive Information tells the host whether the drive supports LBA mode. The host selects LBA mode via the Drive/Head Register. Sector number, Cylinder Low, Cylinder High, and Drive/Head Register bits HS3=0 contain the zero-based LBA. The drive's sectors are linearly mapped with: LBA = 0 => Cylinder 0, head 0, sector 1. Regardless of the translation mode, a sector LBA address does not change. LBA = (Cylinder * no of heads + heads) * (sectors/track) + (Sector - 1).

10 ATA Commands

10.1 Check Power Mode - 98h or E5h

This command checks the current power mode of the adapter. When this command is issued and the adapter is in standby mode, or is being set to standby mode, or during a recovery from standby mode is attempted, adapter sets the BSY bit in the Status register and sets the Sector Count Register to "00H". Then the BSY bit in the Status register is cleared. When the adapter is in the Idle mode, it sets the BSY bit in the Status register and sets "FFH" in the Sector Count Register. Then the BSY bit in the Status register is cleared. An interrupt is issued after the BSY bit is cleared.

INPUTS

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Command	98H or E5H							

OUTPUTS

Register	7	6	5	4	3	2	1	0
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
	V	V	V	V	V			V
Sector Count	Power Mode Code.(00H or 80H or FFH)							
Error	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
						V		

10.2 Execute Drive Diagnostic - 90h

This command performs self-diagnostics on various internal components of the adapter. Results of the test are reported in the Error Register. Note that the bit definitions for the Error Register do not apply with this command. Instead, the value in the Error Register is a diagnostic code, defined in the table below.

INPUTS

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head				DEV				
Command	90H							

OUTPUTS: The diagnostic code written into the Error Register is an 8-bit code as shown in the table below.

Register	7	6	5	4	3	2	1	0
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
	V	V		V				V
Error	Diagnostic code, see table below							

Code	Description
01H	No error detected
02H	Format Media error
03H	Sector buffer error
04H	ECC logic error
05H	Controlling microprocessor error

10.3 Erase Sector(s) - C0h

This command is processed as a NOP command. INPUTS

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	[LBA mode only] The number of sectors to be formatted on the track, must be set to FFh							
Sector Number	[LBA mode only] LBA[7:0] of the first sector/LBA to transfer							
Cylinder Low	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to transfer							
Cylinder High	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to transfer							
Device/Head		LBA		DEV	H[3:0] or LBA[27:24] of the starting sector/LBA			
Command	C0h							

OUTPUTS

Register	7	6	5	4	3	2	1	0
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
	V	V	V	V				V
Error	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	V			V		V		V

10.4 Format Track - 50h

This command is processed as a NOP command.

INPUTS

Register	7	6	5	4	3	2	1	0
Features								
Sector Count	[LBA mode only] The number of sectors to be formatted on the track. Must be set to FFh							
Sector Number	[LBA mode only] LBA[7:0] of the first sector/LBA to transfer							
Cylinder Low	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to transfer							
Cylinder High	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to transfer							
Device/Head		LBA		DEV	H[3:0] or LBA[27:24] of the starting sector/LBA			
Command	50h							

OUTPUTS

Register	7	6	5	4	3	2	1	0
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
	V	V	V	V				V
Error	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
				V		V		V

10.5 Identify Drive - ECh

The Identify Drive command enables the host to receive parameter information from the adapter. When the command is issued, the adapter sets the BSY bit, prepares to transfer the 256 words of adapter identification data to the host, sets the DRQ bit, clears the BSY bit, and generates an interrupt. The host can then transfer the data by reading the Data register. All reserved bits or words are all zero. See following table for the identify drive information for this adapter

INPUTS

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head				DEV				
Command	ECh							

OUTPUTS

Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
Status	V	V	V	V	V			V
	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
Error						V		

Identify Drive Information

Word	Data	Description
0	848Ah	General configuration bit-significant information
1	Note 1	Number of Cylinders
2	0000h	Reserved
3	Note 1	Number of Heads
4	Note 1	Number of unformatted bytes per track
5	2010h	Number of unformatted bytper sector
6	Note 1	Number of sectors per track
7-8	XXXXh	Number of sectors per card (Word 7= MSW, Word 8= LSW)
9	XXXXh	Vendor Unique
10-19	2020h.. ...2020 h	20 ASCII char serial number. Words 10-19 are filled with 20 ASCII ‘space’ chars, 20h
20	0001h	Buffer type: Dual ported, multi-sector, w/ read cache
21	0001h	Buffer size, in 512 byte increments
22	0004h	ECC length
23-26	XXXX	Firmware revision, 8 ASCII chars
27-46	XXXX	Model Number (Vendor Unique)
47	0001h	Maximum Block Count=1 for Read/Write Multiple commands
48	0000h	Cannot perform double word I/O (32 bit)
49	0200h	Capabilities: LBA supported (bit 9), DMA not supported (bit 8)
50	0000h	Reserved
51	0100h	PIO timing mode 1
52	0000h	DMA transfer not supported
53	0001h	Words 54 - 58 are valid
54	Note 1	Number of Current Cylinders
55	Note1	Number of Current Heads
56	Note 1	Number of Current Sectors Per Track
57	Note 1	LSW of the Current Capacity in Sectors
58	Note1	MSW of the Current Capacity in Sectors
59	0100h	Current Setting for Block Count=1 for R/W Multiple commands
60	Note 1	LSW of the total number of user addressable LBA’s
61	Note 1	MSW of the total number of user addressable LBA’s
62-255	0000H ...	Reserved

Note1: Variable by capacity

10.6 Idle - 97h or E3h

Although this command is supported for backward compatibility, it has no actual function. The adapter will always return a 'good' status at the completion of this command.

INPUTS

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Time-out Parameter. This parameter is ignored by the adapter							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head				DEV				
Command	97h or E3h							

OUTPUTS

Register	7	6	5	4	3	2	1	0
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
	V	V	V	V	V			V
Error	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
						V		

10.7 Idle Immediate - 95h or E1h

Although this command is supported for backward compatibility, it has no actual function. The adapter will always return a 'good' status at the completion of this command.

INPUTS

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head				DEV				
Command	95h or E1h							

OUTPUTS

Register	7	6	5	4	3	2	1	0
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
	V	V	V	V	V			V
Error	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
						V		

10.8 Initialize Drive Parameters - 91h

Initialize Drive Parameters allows the host to alter the number of sectors per track and the number of heads per cylinder. This command does not check the validity of counts of sectors and heads. If an invalid value is set, an error will be reported when another command attempts an invalid access.

The Sector Count Register specifies the number of logical sectors per logical track, and the Device/Head register specifies the maximum head number.

INPUTS

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Number of sectors							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head				DEV	Max Head (no. of head = 1)			
Command	91H							

OUTPUTS

Register	7	6	5	4	3	2	1	0
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
	V	V		V	V			V
Error	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF

10.9 Read Buffer - E4h

The Read Buffer command enables the host to read the current contents of the adapter's sector buffer. This command has the same protocol as the Read Sector(s) command.

INPUTS

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head		LBA		DEV				
Command	E4H							

OUTPUTS

Register	7	6	5	4	3	2	1	0
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
	V	V	V	V	V			V
Error	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
						V		

10.10 Read Long Sector(s) - 22h or 23h

Read Long (w/ and w/o retry) is similar to the Read Sectors command, except that the content of the Sector Count Register is ignored and only one sector is read. The 512 data bytes and 4 ECC bytes are read into the buffer (with no ECC correction) and then transferred to the host.

The Cylinder Low, Cylinder High, Device/Head and Sector Number specify the starting sector address to be read. The Sector Count Register shouldn't specify a value other than 1.

INPUTS

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	The number of sectors/logical blocks to transfer. This should be set to 01 for compatibility							
Sector Number	Sector[7:0] or LBA[7:0] of the sector/LBA to transfer							
Cylinder Low	Cylinder[7:0] or LBA[15:8] of the sector/LBA to transfer							
Cylinder High	Cylinder[15:8] or LBA[23:16] of the sector/LBA to transfer							
Device/Head		LBA		DEV	H[3:0] or LBA[27:24] of the sector/LBA to transfer			
Command	22H (retries enabled) or 23H (retries disabled)							

OUTPUTS

Register	7	6	5	4	3	2	1	0
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
	V	V	V	V	V			V
Sector Count	00 if the command proceed without error, else the number of untransfered sectors.							
Sector Number	Sector[7:0] or LBA[7:0] of the last sector read							
Cylinder Low	Cylinder[7:0] or LBA[15:8] of the last sector read							
Cylinder High	Cylinder[15:8] or LBA[23:16] of the last sector read							
Error	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	V			V		V		V

10.11 Read Multiple - C4h

This command functions like the Read Sector(s) command, but instead of issuing interrupts for each sector, interrupts are issued when a block containing the counts of sectors, defined by the Set Multiple command is, transferred. Also, the DRQ required for the transfer only has to be set at the start of the data block and does not affect other sectors. When the Read Multiple command is issued, the requested sectors (not the block counts or the sector counts in a block) are written into the Sector Count Register. Errors occurring during command execution are reported at the start of a block transfer or at the start of transfer of part of a block. However, the transfer continues even if DRQ is set and the data is corrupted. After the data transfer, the content of the task file with the block data containing the sectors where the error occurred is not defined. To obtain valid error information the host has to request a re-transmission. The next block or part of a block is transferred only if the error is correctable. For all other errors the command is aborted after transferring a block containing an error. The Read Multiple command is supported for backward compatibility. If R/W Multiple commands have been enabled by a previous valid Set Multiple command, the Read Multiple command is identical to the Read Sectors operation except that several sectors are transferred as a block to the Host without the intervening Host handshaking. The block count stands for the number of sectors to be transferred as a block. It is established using the Set Multiple command. Although the Set Multiple, and R/W Multiple commands are supported, the only valid block count is one.

INPUTS

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	The number of sectors/logical blocks to transfer							
Sector Number	Sector[7:0] or LBA[7:0] of the sector/LBA to transfer							
Cylinder Low	Cylinder[7:0] or LBA[15:8] of the sector/LBA to transfer							
Cylinder High	Cylinder[15:8] or LBA[23:16] of the sector/LBA to transfer							
Device/Head		LBA		DEV	Head number or LBA			
Command	C4H							

OUTPUTS

Register	7	6	5	4	3	2	1	0
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
	V	V	V	V	V	V		V
Sector Count	The first sector where the first unrecoverable error occurred							
Sector Number	Sector[7:0] or LBA[7:0] of the last good sector transferred							
Cylinder Low	Cylinder[7:0] or LBA[15:8] of the last good sector transferred							
Cylinder High	Cylinder[15:8] or LBA[23:16] of the last good sector transferred							
Device/Head		LBA		DEV	H[3:0] or LBA[27:24] last good sector transferred			
Error	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	V	V	V	V	V	V	V	V

10.12 Read Sectors(s) - 20 or 21h

The Cylinder Low, Cylinder High, Device/Head and Sector Number or LBA registers specify the starting sector address to be read. The Sector Count Register specifies the number of sectors to be transferred.

INPUTS

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	The number of sectors/logical blocks to transfer							
Sector Number	Sector[7:0] or LBA[7:0] of the sector/LBA to transfer							
Cylinder Low	Cylinder[7:0] or LBA[15:8] of the sector/LBA to transfer							
Cylinder High	Cylinder[15:8] or LBA[23:16] of the sector/LBA to transfer							
Device/Head		LBA		DEV	H[3:0] or LBA[27:24] of the sector/LBA to transfer			
Command	20H (retry enabled) or 21H (retries disabled)							

OUTPUTS

Register	7	6	5	4	3	2	1	0
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
	V	V	V	V	V	V		V
Sector Count	The first sector where the first unrecoverable error occurred							
Sector Number	Sector[7:0] or LBA[7:0] of the last good sector transferred							
Cylinder Low	Cylinder[7:0] or LBA[15:8] of the last good sector transferred							
Cylinder High	Cylinder[15:8] or LBA[23:16] of the last good sector transferred							

Device/Head		LBA		DEV	H[3:0] or LBA[27:24] last good sector transferred			
Error	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	V	V	V	V	V	V		V

10.13 Read Verify Sector(s) - 40 or 41h

The Read Verify Sectors command verifies one or more sectors on the card by transferring data from the Flash media to the data buffer in the card and verifying that the ECC is correct. It is performed identically to the Read Sectors command, except that DRQ is not asserted, and no data is transferred to the host. If an uncorrectable error occurs, the Read Verify command will be terminated at the failing sector. The task file registers contain the CHS, or LBA of the sector in which the error occurred.

The Cylinder Low, Cylinder High, Device/Head and Sector Number specify the starting sector address to be verified. The Sector Count Register specifies the number of sectors to be verified.

INPUTS

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	The number of sectors/logical blocks to verify							
Sector Number	Sector[7:0] or LBA[7:0] of the first sector/LBA to verify							
Cylinder Low	Cylinder[7:0] or LBA[15:8] of the sector/LBA to verify							
Cylinder High	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to verify							
Device/Head		LBA		DEV	H[3:0] or LBA[27:24] of the sector/LBA to verify			
Command	40H (retries enabled) or 41H (retries disabled)							

OUTPUTS

Register	7	6	5	4	3	2	1	0
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
	V	V	V	V	V	V		V
Sector Count	The first sector where the first unrecoverable error occurred							
Sector Number	Sector[7:0] or LBA[7:0] of the sector/LBA to transfer							
Cylinder Low	Cylinder[7:0] or LBA[15:8] of the sector/LBA to transfer							
Cylinder High	Cylinder[15:8] or LBA[23:16] of the last good sector transferred							
Device/Head		LBA		DEV	H[3:0] or LBA[27:24] of the sector/LBA to transfer			
Error	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	V	V	V	V	V	V		V

10.14 Recalibrate - 1Xh

The adapter performs only the interface timing and register operations. When this command is issued, the adapter sets BSY and waits for an appropriate length of time after which it clears BSY and issues an interrupt. When this command ends normally, the adapter is initialized.

INPUTS

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head				DEV				
Command	1XH							

OUTPUTS

Register	7	6	5	4	3	2	1	0
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
		V	V	V				V
Error	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
						V		

10.15 Request Sense - 03h

This command requests extended error information for the previous command. The table below defines the valid extended error codes. Those codes are placed in the Error Register.

INPUTS

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head				DEV				
Command	03H							

OUTPUTS

The diagnostic code written into the Error Register is an 8-bit code as shown in the table below.

Register	7	6	5	4	3	2	1	0
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
	V	V		V				V
Error	Sense code, see table below							

Code	Description
00H	No error detected
01H	Self test OK (No error)
03H	Write/Erase failed
09H	Miscellaneous Error - N/A
20H	Invalid Command
21H	Invalid Address (requested Head or Sector invalid)
2FH	Address Overflow (address too large)
35H, 36H	Supply or generate Voltage Out of Tolerance
11H	Uncorrectable ECC Error
18H	Corrected ECC Error - N/A
05H, 30H-34H, 37H, 3EH	Self Test Diagnostic Failed
10H, 14H	ID Not Found - N/A
3AH	Spare Sectors Exhausted
1FH	Data Transfer Error / Aborted Command
0CH, 38H, 3BH, 3CH, 3FH	Corrupted Media Format - N/A

10.16 Seek - 7Xh

This command seeks and picks up the head to track specified in the Task File registers. Actually the adapter performs only an interface timing and register information.

INPUTS

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	(Valid in LBA mode only) LBA[7:0] of the track							
Cylinder Low	Cylinder[7:0] or LBA[15:8] of the track							
Cylinder High	Cylinder[15:8] or LBA[23:16] of the track							
Device/Head		LBA		DEV	H[3:0] or LBA[27:24] of the track			
Command	7XH							

OUTPUTS

Register	7	6	5	4	3	2	1	0
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
	V	V	V	V	V			V
Error	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
			V	V	V	V		

10.17 Set Feature - EFh

This command is used by the host to establish or select from the specific features listed below.(after a power up or a hardware reset) An ATA software reset does not set the features to default. The feature code is set to 81H, this mode is the default mode.

INPUTS

Register	7	6	5	4	3	2	1	0
Features	Feature number according to the table below							
Sector Count	Configuration required							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head				DEV				
Command	EFH							

Feature Codes

Code	Description
01h	Enable 8-bit data transfers
55h	Disable Read Look Ahead
66h	Disable reverting to power on defaults
81h	Disable 8-bit data transfers
BBh	4 bytes of ECC apply on read long/write long commands
CCh	Enable reverting to power on defaults

OUTPUTS

Register	7	6	5	4	3	2	1	0
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
	V	V	V	V	V			V
Error	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
						V		

10.18 Set Multiple Mode - C6h

The Set Multiple command allows the adapter to perform Read Multiple and Write Multiple operations. It also sets the block count (counts of sectors making up a block) for these commands. The sector count per block is placed is the Sector Count Register. The adapter supports only blocks with one sector.

INPUTS

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Sector Count per Block(= 1)							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head				DEV				
Command	C6H							

OUTPUTS

Register	7	6	5	4	3	2	1	0
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
	V	V	V	V	V			V
Error	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
						V		

10.19 Set Sleep Mode - 99h or E6h

This is the only command that allows the host to set the adapter into Sleep mode. When the adapter is set to sleep mode, the adapter clears the BSY line and issues an interrupt. The adapter enters sleep mode and the only method to make the adapter active again (back to normal operation) is by performing a hardware reset or software reset.

INPUTS

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head				DEV				
Command	99H/E6H							

OUTPUTS

Register	7	6	5	4	3	2	1	0
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
	V	V	V	V	V			V
Error	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
						V		

10.20 Standby - 96h or E2h

This command is sets the adapter in Standby mode. If the Sector Count Register is a value other than 0H, an Auto Power Down is enabled and when the adapter returns to the idle mode, the timer starts a countdown. The time is set in the Sector Count Register.

INPUTS

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Time period value							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head				DEV				
Command	96H or E2H							

OUTPUTS

Register	7	6	5	4	3	2	1	0
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
	V	V	V	V	V			V
Error	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
						V		

10.21 Standby Immediate 94h or E0h

This command sets the adapter into standby mode.

INPUTS

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head				DEV				
Command	94H or E0h							

OUTPUTS

Register	7	6	5	4	3	2	1	0
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
	V	V	V	V	V			V
Error	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
						V		

10.22 Translate Sector - 87h

This command allows the host a method of determining the exact number of times a sector was used (erased). The controller responds with the 512-byte buffer of information that includes the Hot Count, if available, for the sector. This command is not supported in this adapter and will always return the Hot Count as “00”.

INPUTS

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Sector Count							
Sector Number	Sector[7:0] or LBA[7:0] of the first sector/LBA to transfer							
Cylinder Low	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to transfer							
Cylinder High	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to transfer							
Device/Head		LBA		DEV	H[3:0] or LBA[27:24] of the starting sector/LBA			
Command	87H							

OUTPUTS

The diagnostic code written into the Error Register is an 8-bit code as shown in the table below.

Register	7	6	5	4	3	2	1	0
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
	V	V	V	V				V
Error	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	V			V		V		

Address	Information
00H - 01H	Cylinder MSB (00H), Cylinder LSB (01H)
02H	Head
03H	Sector
04H - 06H	LBA MSB (04H) - LSB (06H)
07H - 12H	Reserved
13H	Erased Flag (FFH) = Erased; (00H) = Not Erased
14H - 17H	Reserved
18H - 1AH	Hot Count MSB (18H) - LSB (1AH)
1BH - 1FFH	Reserved

10.23 Wear Level - F5h

This command is effectively a NOP command and only implemented for backward compatibility. The Sector Count Register will always return the value “00H”, indicating that wear leveling is not needed.

INPUTS

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head				DEV				
Command	F5H							

OUTPUTS

Register	7	6	5	4	3	2	1	0
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
	V	V	V	V	V			V
Sector Count	Always “00H”							
Error	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	V	V	V	V	V	V		V

10.24 Write Buffer - E8h

This command enables the host to rewrite the contents of the adapter data buffer in the adapter with the desired data sting. This data buffer can be accessed by and read by the Read Buffer Command.

INPUTS

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head				DEV				
Command	E8H							

OUTPUTS

Register	7	6	5	4	3	2	1	0
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
	V	V	V	V	V			V
Error	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
						V		

10.25 Write Long Sector(s) 32h or 33h

This command operates in the same way as the Write Sector command except that it writes data and ECC bytes for long commands directly from the sector buffer. ECC bytes for long commands are byte writes that consist of a 4-byte fixed length data. This command can write only one sector at a time.

INPUT

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	“01h”							
Sector Number	Sector[7:0] or LBA[7:0] of the first sector/LBA to transfer							
Cylinder Low	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to transfer							
Cylinder High	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to transfer							
Device/Head		LBA		DEV	H[3:0] or LBA[27:24] of the starting sector/LBA			
Command	32H or 33H							

OUTPUTS

Register	7	6	5	4	3	2	1	0
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
	V	V	V	V	V			V
Sector Count	Bit-0 if the command proceeded successfully, other – untransferred sectors count							
Sector Number	Sector[7:0] or LBA[7:0] of the last good sector transferred							
Cylinder Low	Cylinder[7:0] or LBA[15:8] of the last good sector transferred							
Cylinder High	Cylinder[15:8] or LBA[23:16] of the last good sector transferred							
Error	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	V			V		V		

10.26 Write Multiple - C5h

This command functions in the same way as the Write Sector command. When this command is issued, the adapter sets the BSY within 400nsec. Interrupts are not issued for every sector but after one block consisting of the counts of sectors defined by the Set Multiple command is transferred. The DRQ required for the transfer only has to be set at the beginning of the block and does not affect other sectors.

INPUTS

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Sector Count							
Sector Number	Sector[7:0] or LBA[7:0] of the first sector/LBA to transfer							
Cylinder Low	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to transfer							
Cylinder High	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to transfer							
Device/Head		LBA		DEV	H[3:0] or LB[27:24] of the starting sector/LBA			
Command	C5H							

OUTPUTS

Register	7	6	5	4	3	2	1	0
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
	V	V	V	V	V			V
Sector Count	Bit-0 if the command proceeded successfully, other – untransferred sectors count							
Sector Number	Sector[7:0] or LBA[7:0] of the last good sector transferred							

Cylinder Low	Cylinder[7:0] or LBA[15:8] of the last good sector transferred							
Cylinder High	Cylinder[15:8] or LBA[23:16] of the last good sector transferred							
Error	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	V		V	V	V	V		V

10.27 Write Multiple without Erase - CDh

This command is similar to the Write Multiple command with the exception that an implied erase before using this command. Please note that before using this command it is required to erase the respective sectors using the Erase Sector command.

INPUTS

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Sector Count							
Sector Number	Sector[7:0] or LBA[7:0] of the first sector/LBA to transfer							
Cylinder Low	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to transfer							
Cylinder High	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to transfer							
Device/Head		LBA		DEV	H[3:0] or LB[27:24] of the starting sector/LBA			
Command	CDH							

OUTPUTS

Register	7	6	5	4	3	2	1	0
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
	V	V	V	V	V			V
Sector Count	Bit-0 if the command proceeded successfully, other – untransferred sectors count							
Sector Number	Sector[7:0] or LBA[7:0] of the last good sector transferred							
Cylinder Low	Cylinder[7:0] or LBA[15:8] of the last good sector transferred							
Cylinder High	Cylinder[15:8] or LBA[23:16] of the last good sector transferred							
Error	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	V		V	V	V	V		V

10.28 Write Sector(s) - 30h or 31h

This command allows the host to write the specified number (1 to 256) of sectors in the Sector Count Register. A sector count of 0 indicates a write request of 256 sectors. The write operation starts from the sector specified in the Sector Number register. The command ends execution by placing the cylinder, head and sector number of the last written sector in the Task File registers.

INPUTS

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Sector Count							
Sector Number	Sector[7:0] or LBA[7:0] of the first sector/LBA to transfer							
Cylinder Low	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to transfer							
Cylinder High	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to transfer							
Device/Head		LBA		DEV	H[3:0] or LBA[27:24] of the starting sector/LBA			
Command	30H or 31H							

OUTPUTS

Register	7	6	5	4	3	2	1	0
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
	V	V	V	V	V			V
Sector Count	Bit-0 if the command proceeded successfully, other – untransferred sectors count							
Sector Number	Sector[7:0] or LBA[7:0] of the last good sector transferred							
Cylinder Low	Cylinder[7:0] or LBA[15:8] of the last good sector transferred							
Cylinder High	Cylinder[15:8] or LBA[23:16] of the last good sector transferred							
Error	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	V		V	V	V	V		V

10.29 Write Sector(s) without Erase - 38h

This command is similar to the Write Sector command with the exception that an implied erase before using this command. Please note that before using this command it is required to erase the respective sectors using the Erase Sector command.

` INPUTS

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Sector Count							
Sector Number	Sector[7:0] or LBA[7:0] of the first sector/LBA to transfer							
Cylinder Low	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to transfer							
Cylinder High	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to transfer							
Device/Head		LBA		DEV	H[3:0] or LBA[27:24] of the starting sector/LBA			
Command	38H							

OUTPUTS

Register	7	6	5	4	3	2	1	0
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
	V	V	V	V	V			V
Sector Count	Bit-0 if the command proceeded successfully, other – untransferred sectors count							
Sector Number	Sector[7:0] or LBA[7:0] of the last good sector transferred							
Cylinder Low	Cylinder[7:0] or LBA[15:8] of the last good sector transferred							
Cylinder High	Cylinder[15:8] or LBA[23:16] of the last good sector transferred							
Error	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	V			V		V		V

10.30 Write Verity - 3Ch

This command is similar to the Write Sector command with the exception that each sector is verified immediately after writing.

INPUTS

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Sector Count							
Sector Number	Sector[7:0] or LBA[7:0] of the first sector/LBA to transfer							
Cylinder Low	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to transfer							
Cylinder High	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to transfer							

Device/Head		LBA		DEV	H[3:0] or LBA[27:24] of the starting sector/LBA
Command	3CH				

OUTPUTS

Register	7	6	5	4	3	2	1	0
Status	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
	V	V	V	V	V			V
Sector Count	Bit-0 if the command proceeded successfully, other – untransferred sectors count							
Sector Number	Sector[7:0] or LBA[7:0] of the last good sector transferred							
Cylinder Low	Cylinder[7:0] or LBA[15:8] of the last good sector transferred							
Cylinder High	Cylinder[15:8] or LBA[23:16] of the last good sector transferred							
Error	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	V			V		V		V

10.31 error Posting

Command	Error Register					Status Register				
	BBK	UNC	IDNF	ABRT	AMNF	DRDY	DWF	DSC	CORR	ERR
Check Power Mode				✓		✓	✓	✓		✓
Execute Drive Diagnostic						✓		✓		✓
Erase Sector(s)	✓		✓	✓	✓	✓	✓	✓		✓
Format Track			✓	✓	✓	✓	✓	✓		✓
Identify Drive				✓		✓	✓	✓		✓
Idle				✓		✓	✓	✓		✓
Idle immediate				✓		✓	✓	✓		✓
Initialize Drive Parameter						✓		✓		✓
Read Buffer				✓		✓	✓	✓		✓
Read Multiple	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Read Long Sector	✓		✓	✓	✓	✓	✓	✓		✓
Read Sector(s)	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Read Verify Sectors	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Recalibrate				✓		✓	✓	✓		✓
Request Sense				✓		✓		✓		✓
Security Disable Password				✓		✓	✓	✓		✓
Security Erase Prepare				✓		✓	✓	✓		✓
Security Erase Unit				✓		✓	✓	✓		✓
Security Freeze Lock				✓		✓	✓	✓		✓
Security Set Password				✓		✓	✓	✓		✓
Security Unlock				✓		✓	✓	✓		✓
Seek		✓		✓		✓	✓	✓		✓
Set Features				✓		✓	✓	✓		✓
Set Multiple Mode				✓		✓	✓	✓		✓
Set Sleep Mode				✓		✓	✓	✓		✓
Stand By				✓		✓	✓	✓		✓
Stand By Immediate				✓		✓	✓	✓		✓
Translate Sector	✓		✓	✓	✓	✓	✓	✓		✓
Wear Level	✓	✓	✓	✓	✓	✓	✓	✓		✓
Write Buffer				✓		✓	✓	✓		✓
Write Long Sector	✓		✓	✓	✓	✓	✓	✓		✓
Write Multiple	✓		✓	✓	✓	✓	✓	✓		✓
Write Multiple w/o Erase	✓		✓	✓	✓	✓	✓	✓		✓
Write Sector(s)	✓		✓	✓	✓	✓	✓	✓		✓
Write Sector w/o Erase	✓		✓	✓	✓	✓	✓	✓		✓
Write Verify	✓		✓	✓	✓	✓	✓	✓		✓
Invalid command Code				✓		✓	✓	✓		✓

11. ATA Protocol Overview

Command classes are grouped according to protocols described for command execution. For all commands, the host must first check for BYS=0 before proceeding further. For most commands, the host should not proceed until DRDY=1.

11.1 PIO Data In Commands

Execution includes one more 512 bytes data-sector drive-to-host transfer. If the drive presents error status, it prepares to transfer data at the host's discretion. The host writes parameters to the Feature, Sector Count, Sector Number, Cylinder, and Drive/Head register. The host writes the Command Register's command code. The drive sets BSY and prepares for data transfer when a data sector is available; the drive sets DRQ, clears BSY, and asserts interrupt. At interrupt, the host reads the Status register, the drive negates interrupt, and the host reads one data-sector from Data Register. The drive clears DRQ. If another sector is required, the drive sets BSY and repeats the data transfer from 4.

11.2 PIO Data Out Commands

Execution includes one or more 512 bytes host-to-drive data-sector transfers. The host writes parameters to the Features, Sector Count, Sector Number, Cylinder, and Drive/Head Registers. The host writes the Command register's command code. The drive sets DRQ when it can accept the first sector of data

The host writes one sector of data to the Data register. The Drive clears DRQ and sets BSY. At sector processing complete, the drive clears BSY and asserts interrupt. If another sector transfer is required, the drive also sets DRQ. The host reads the Status register after detecting interrupt. The drive negates the interrupt if another sector transfer is required, the sequence repeats from 4.

11.3 Non Data Commands

Command execution involves no data transfer. The host writes parameters to the Features, Sector Count, Sector Number, Cylinder, and Drive/Head registers. The host writes the Command register's command code. The Drive sets BSY. When the drive completes sector processing, it clears BSY and asserts interrupt. The host reads the Status register after detecting interrupts the drive negates the interrupt.