2 MEGABYTE through 40 MEGABYTE (AMD based)

FEATURES

- Low cost High Density Linear Flash Card
- Supports 5V only systems
- Based on AMD Flash Components
  - low standby power without entering reset mode
  - allows standard access from standby mode
- Fast Read Performance
  - 150ns Maximum Access Time
- x8/ x16 Data Interface
- High Performance Random Writes
  - 10µs Typical Word Write Time
- Automated Write and Erase Algorithms
  - AMD Command Set
- 100,000 Erase Cycles per Block
- 64K word symmetrical Block Architecture
- PC Card Standard Type I Form Factor

GENERAL DESCRIPTION

WEDC's PCMCIA Flash memory cards offer high density linear Flash solid state storage solutions for code and data storage, high performance disk emulation and execute in place (XIP) applications in mobile PC and dedicated (embedded) equipment.

Packaged in PCMCIA type I housing, each card contains a connector, an array of Flash memories packaged in TSOP packages and card control logic. The card control logic provides the system interface and controls the internal Flash memories. Combined with file management software, such as Flash Translation Layer (FTL), WEDC Flash cards provide removable high-performance disk emulation.

The WEDC FLA series is based on AMD Flash memories. The FLB series offers byte wide and word wide operation, low power modes and Card Information Structure (CIS) for easy identification of card characteristics.

Note: Standard options include attribute memory. Cards without attribute memory are available. Cards are also available with or without a hardware write protect switch.

ARCHITECTURE OVERVIEW

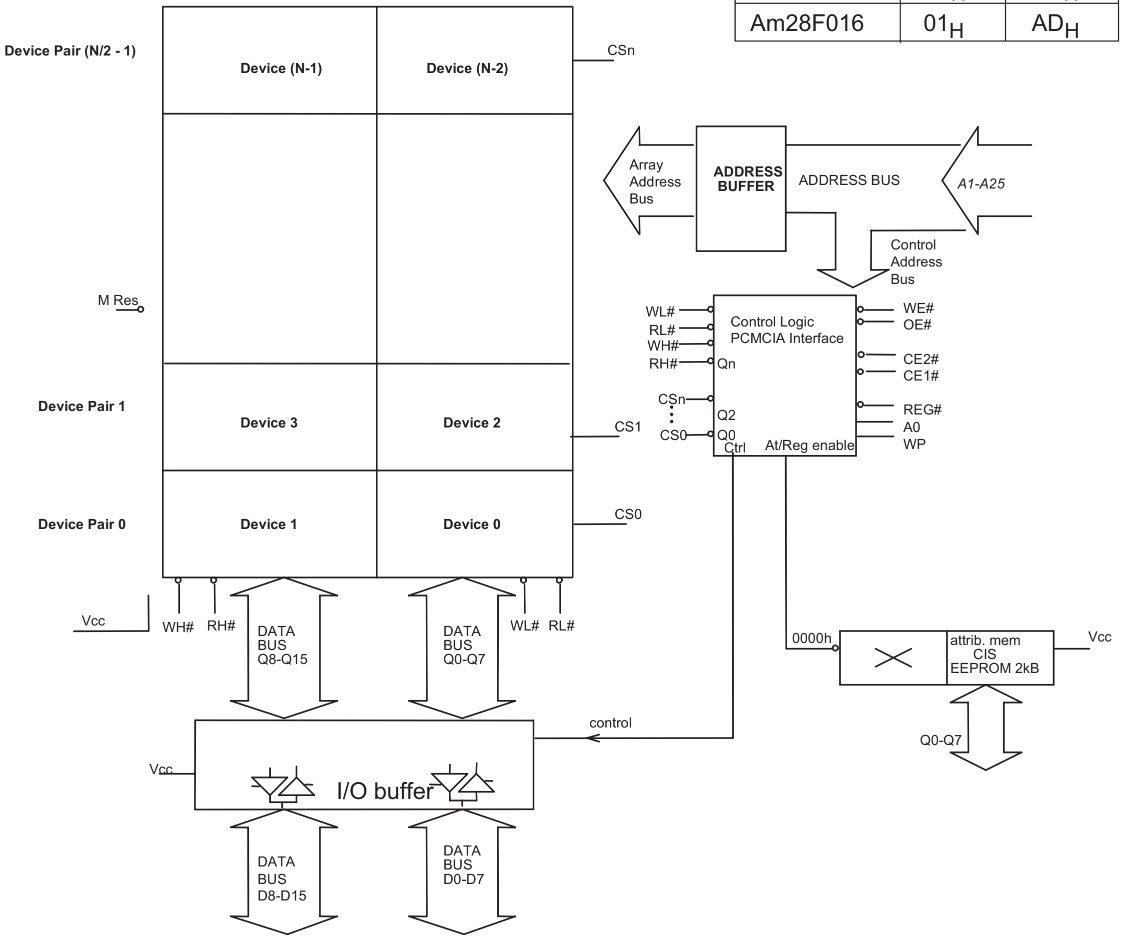
WEDC's FLB series is designed to support from two to twenty (see Block diagram) 8Mb or 16MB components, providing a wide range of density options. Cards are based on the Am29F080 (8Mb) or Am29F016 (16Mb) devices for 5V only applications. Devices codes for the Am29F080 and Am29F016 are D5H and ADH respectively. Systems should be able to recognize both codes. Cards utilizing the 8Mb components provide densities ranging from 2MB to 20MB in 2MB increments, cards utilizing 16Mb components provide densities ranging from 4MB to 40MB in 4MB increments.

In support of the PC Card 95 standard for word wide access devices are paired. Therefore, the Flash array is structured in 64K word blocks. Write, read and block erase operations can be performed as either a word or byte wide operation . By multiplexing A0, CE1# and CE2#, 8-bit hosts can access all data on data lines DQ0 - DQ7. The FLB series cards conform with the PC Card Standard (formerly PCMCIA) and supported JEIDA, providing electrical and physical compatibility. The PC Card form factor offers an industry standard pinout and mechanical outline, allowing density upgrades without system design changes.

WEDC's standard cards are shipped with WEDC's silkscreen design. Cards are also available with blank housings (no silkscreen). The blank housings are available in both a recessed (for label) and flat housing. Please contact WEDC sales representative for further information on Custom artwork.

BLOCK DIAGRAM

Device type	Manuf ID	Device ID
Am28F080	01_H	$D5_H$
Am28F016	01_H	AD_H



PINOUT

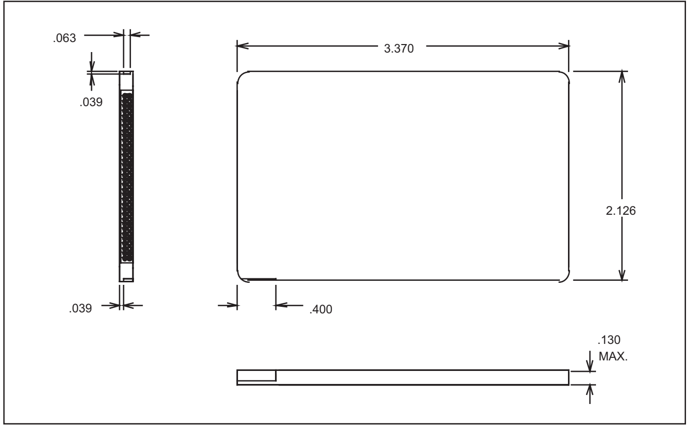
Pin	Signal name	I/O	Function	Active
1	GND		Ground	
2	DQ3	I/O	Data bit 3	
3	DQ4	I/O	Data bit 4	
4	DQ5	I/O	Data bit 5	
5	DQ6	I/O	Data bit 6	
6	DQ7	I/O	Data bit 7	
7	CE1#	I	Card enable 1	LOW
8	A10	I	Address bit 10	
9	OE#	I	Output enable	LOW
10	A11	I	Address bit 11	
11	A9	I	Address bit 9	
12	A8	I	Address bit 8	
13	A13	I	Address bit 13	
14	A14	I	Address bit 14	
15	WE#	I	Write Enable	LOW
16	RDY/BSY#	O	Ready/Busy	LOW
17	VCC		Supply Voltage	
18	VPP1		Prog. Voltage	N.C.
19	A16	I	Address bit 16	
20	A15	I	Address bit 15	
21	A12	I	Address bit 12	
22	A7	I	Address bit 7	
23	A6	I	Address bit 6	
24	A5	I	Address bit 5	
25	A4	I	Address bit 4	
26	A3	I	Address bit 3	
27	A2	I	Address bit 2	
28	A1	I	Address bit 1	
29	A0	I	Address bit 0	
30	DQ0	I/O	Data bit 0	
31	DQ1	I/O	Data bit 1	
32	DQ2	I/O	Data bit 2	
33	WP	O	Write Potect	HIGH
34	GND		Ground	

Pin	Signal name	I/O	Function	Active
35	GND		Ground	
36	CD1#	O	Card Detect 1	LOW
37	DQ11	I/O	Data bit 11	
38	DQ12	I/O	Data bit 12	
39	DQ13	I/O	Data bit 13	
40	DQ14	I/O	Data bit 14	
41	DQ15	I	Data bit 15	
42	CE2#	I	Card Enable 2	LOW
43	VS1	O	Voltage Sense 1	N.C.
44	RFU		Reserved	
45	RFU		Reserved	
46	A17	I	Address bit 17	
47	A18	I	Address bit 18	
48	A19	I	Address bit 19	
49	A20	I	Address bit 20	2MB(2)
50	A21	I	Address bit 21	4MB(2.3)
51	VCC		Supply Voltage	
52	VPP2		Prog. Voltage	NC
53	A22	I	Address bit 22	8MB(3)
54	A23	I	Address bit 23	16MB(3)
55	A24	I	Address bit 24	32MB(3)
56	A25	I	Address bit 25	64MB(3)
57	VS2	O	Voltage Sense 2	N.C.
58	RST	I	Card Reset	HIGH
59	Wait#	O	Extended Bus cycle	LOW(2)
60	RFU		Reserved	
61	REG#	I	Attrib Mem Select	
62	BVD2	O	Bat. Volt. Detect 2	(2)
63	BVD1	O	Bat. Volt. Detect 1	(2)
64	DQ8	I/O	Data bit 8	
65	DQ9	I/O	Data bit 9	
66	DQ10	O	Data bit 10	
67	CD2#	O	Card Detect 2	LOW
68	GND		Ground	

Notes:

1. RDY/BSY is an open drain output, external pull-up resistor is required.
2. Wait#, BVD1 and BVD2 are driven high for compatibility.
3. Shows density for which specified address bit is MSB. Higher order address bits are no connects (ie 4MB A21 is MSB A22 - A25 are NC).

MECHANICAL



CARD SIGNAL DESCRIPTION

Symbol	Type	Name and Function
A0 - A25	INPUT	**ADDRESS INPUTS:** A0 through A25 enable direct addressing of up to 64MB of memory on the card. Signal A0 is not used in word access mode. The memory will wrap at the card density boundary (see PINOUT, note 3). The system should not try to access memory beyond the card density. A25 is the most significant bit. A24 – A25 are not connected.
DQ0 - DQ15	INPUT/OUTPUT	**DATA INPUT/OUTPUT:** DQ0 THROUGH DQ15 constitute the bi-directional databus. DQ0 – DQ7 constitute the lower (even) byte and DQ8 – DQ15 the upper (odd) byte. DQ15 is the MSB.
CE1#, CE2#	INPUT	**CARD ENABLE 1 AND 2:** CE1# enables even byte accesses, CE2# enables odd byte accesses. Multiplexing A0, CE1# and CE2# allows 8-bit hosts to access all data on DQ0 - DQ7.
OE#	INPUT	**OUTPUT ENABLE:** Active low signal gating read data from the memory card.
WE#	INPUT	**WRITE ENABLE:** Active low signal gating write data to the memory card.
RDY/BSY#	N.C.	**READY/BUSY OUTPUT:** Indicates status of internally timed erase or program algorithms. This signal is not connected.
CD1#, CD2#	OUTPUT	**CARD DETECT 1 and 2:** Provide card insertion detection. These signals are internally connected to ground on the card. The host shall monitor these signals to detect card insertion (pulled-up on host side).
WP	OUTPUT	**WRITE PROTECT:** Write protect reflects the status of the Write Protect switch on the memory card. WP set to high = write protected, providing internal hardware write lockout to the Flash array. If card does not include optional write protect switch, this signal will be pulled low internally indicating write protect = “off”.
VPP1	N.C.	**PROGRAM/ERASE POWER SUPPLY:** Provides programming voltages 12.0V for lower byte (D0 – D7) memory components. This signal is not connected.
VPP2	N.C.	**PROGRAM/ERASE POWER SUPPLY:** Provides programming voltages 12.0V for upper byte (D8 – D15) memory components. This signal is not connected.
VCC		**CARD POWER SUPPLY:** (5.0V).
GND		**CARD GROUND**
REG#	INPUT	**ATTRIBUTE MEMORY SELECT:** Active low signal, enables access to Attribute Memory Plane, occupied by Card Information Structure and Card Registers.
RST	N.C.	**RESET:** Active high signal for placing cards in Power-on default state. This signal is not connected.
WAIT#	OUTPUT	**WAIT:** This signal is pulled high internally for compatibility. No wait states are generated.
BVD1, BVD2	OUTPUT	**BATTERY VOLTAGE DETECT:** These signals are pulled high to maintain SRAM card compatibility.
VS1, VS2	OUTPUT	**VOLTAGE SENSE:** Notifies the host socket of the card’s V_{CC} requirements. VS1 and VS2 are open to indicate a 5V card.
RFU		**RESERVED FOR FUTURE USE**
N.C.		**NO INTERNAL CONNECTION TO CARD:** pin may be driven or left floating

CARD SIGNAL DESCRIPTION

Symbol	Type	Name and Function
A0 - A25	INPUT	**ADDRESS INPUTS:** A0 through A25 enable direct addressing of up to 64MB of memory on the card. Signal A0 is not used in word access mode. A25 is the most significant bit
DQ0 - DQ15	INPUT/ OUTPUT	**DATA INPUT/OUTPUT:** DQ0 THROUGH DQ15 constitute the bi-directional databus. DQ15 is the MSB.
CE1#, CE2#	INPUT	**CARD ENABLE 1 AND 2:** CE1# enables even byte accesses, CE2# enables odd byte accesses. Multiplexing A0, CE1# and CE2# allows 8-bit hosts to access all data on DQ0 - DQ7.
OE#	INPUT	**OUTPUT ENABLE:** Active low signal gating read data from the memory card.
WE#	INPUT	**WRITE ENABLE:** Active low signal gating write data to the memory card.
RDY/BSY#	OUTPUT	**READY/BUSY OUTPUT:** Indicates status of internally timed erase or program algorithms. A high output indicates that the card is ready to accept accesses. A low output indicates that one or more devices in the memory card are busy with internally timed erase or write activities.
CD1#, CD2#	OUTPUT	**CARD DETECT 1 and 2:** Provide card insertion detection. These signals are connected to ground internally on the memory card. The host socket interface circuitry shall supply 10K-ohm or larger pull-up resistors on these signal pins.
WP	OUTPUT	**WRITE PROTECT:** Write protect reflects the status of the Write Protect switch on the memory card. WP set to high = write protected, providing internal hardware write lockout to the Flash array. If card does not include optional write protect switch, this signal will be pulled low internally indicating write protect = “off”.
VPP1, VPP2	N.C.	**PROGRAM/ERASE POWER SUPPLY:** Not connected for 5V only card.
VCC		**CARD POWER SUPPLY:** 5.0V for all internal circuitry.
GND		**GROUND:** for all internal circuitry.
REG#	INPUT	**ATTRIBUTE MEMORY SELECT:** provides access to Flash memory card registers and Card Information Structure in the Attribute Memory Plane.
RST	INPUT	**RESET:** Active high signal for placing card in Power-on default state. Reset can be used as a Power-Down signal for the memory array.
WAIT#	OUTPUT	**WAIT:** This signal is pulled high internally for compatibility. No wait states are generated.
BVD1, BVD2	OUTPUT	**BATTERY VOLTAGE DETECT:** These signals are pulled high to maintain SRAM card compatibility.
VS1, VS2	OUTPUT	**VOLTAGE SENSE:** Notifies the host socket of the card’s VCC requirements. VS1 and VS2 are open to indicate a 5V card has been inserted.
RFU		**RESERVED FOR FUTURE USE**
N.C.		**NO INTERNAL CONNECTION TO CARD:** pin may be driven or left floating

ABSOLUTE MAXIMUM RATINGS (2)

Operating Temperature T_A (ambient)	
Commercial	0°C to +60°C
Industrial	-40°C to +85°C**
Storage Temperature	
Commercial	-30°C to +80°C
Industrial	-40°C to +85°C**
Voltage on any pin relative to V_{SS}	-0.5V to V_{CC}+0.5V (1)
V_{CC} supply Voltage relative to V_{SS}	-0.5V to +7.0V

** Advanced information

Notes:

1. During transitions, inputs may undershoot to -2.0V or overshoot to V_{CC} +2.0V for periods less than 20ns.
2. Stress greater than those listed under “Absolute Maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC CHARACTERISTICS (1)

Symbol	Parameter	Density	Notes	Typ(4)	Max	Units	Test Conditions
I_{CCR}	V_{CC} Read Current	All			75	mA	V_{CC} = V_{CC} max tcycle = 150ns, CMOS levels
I_{CCW}	V_{CC} Program Current	All			150	mA	
I_{CCE}	V_{CC} Erase Current	All			150	mA	
I_{CCS} (CMOS)	V_{CC} Standby Current	1MB (4MB)	2,3	80	230	mA	V_{CC} = V_{CC} max Control Signals = V_{CC} CMOS levels

CMOS Test Conditions: V_{CC} = 5V ± 5%, V_{IL} = V_{SS} ± 0.2V, V_{IH} = V_{CC} ± 0.2V

Notes:

1. All currents are RMS values unless otherwise specified. ICCR, ICCW and ICCE are based on Word wide operations.
2. Control Signals: CE1#, CE2#, OE#, WE#, REG#.
3. I_{CCD} and I_{CCS} are specified for lowest density card for each component type (2MB for 8Mb components and 4MB for 16Mb components) This represents a single pair of devices. For higher densities multiply the number of device pairs by the specified current in the table. For example a 40MB card will use 10 device pairs of 16Mb components. The maximum I_{CCD} will be 10 x 40µA = 400µA. The maximum I_{CCS} will be 10 x 230µA = 2.3mA.
4. Typical: V_{CC} = 5V, T = +25°C.

Symbol	Parameter	Notes	Min	Max	Units	Test Conditions
I_{LI}	Input Leakage Current	1		±20	µA	V_{CC} = V_{CC}MAX V_{IN} =V_{CC} or V_{SS}
I_{LO}	Output Leakage Current	1		±20	µA	V_{CC} = V_{CC}MAX V_{OUT} =V_{CC} or V_{SS}
V_{IL}	Input Low Voltage	1	0	0.8	V	
V_{IH}	Input High Voltage	1	0.7V_{CC}	V_{CC}+0.5	V	
V_{OL}	Output Low Voltage	1		0.4	V	I_{OL} = 3.2mA
V_{OH}	Output High Voltage	1	V_{CC}-0.4	V_{CC}	V	I_{OH} = -2.0mA
V_{LKO}	V_{CC} Erase/Program Lock Voltage	1	2.0		V	

Notes:

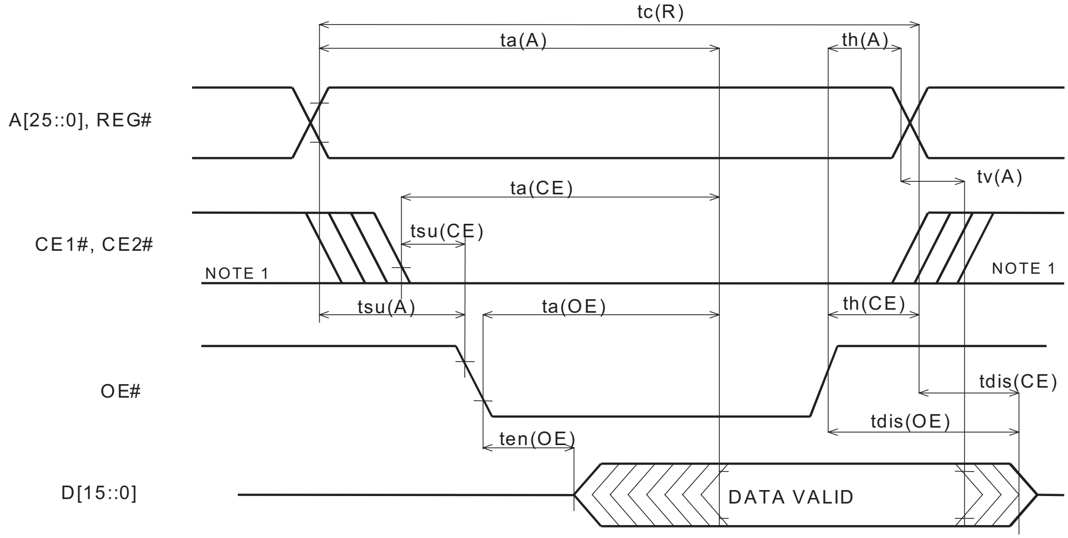
1. Values are the same for byte and word wide modes for all card densities.
2. Exceptions: Leakage currents on CE1#, CE2#, OE#, REG# and WE# will be < 500 µA when V_{IN} = GND due to internal pull-up resistors.
   Leakage currents on RST will be <150µA when V_{IN}=V_{CC} due to internal pull-down resistor.

AC CHARACTERISTICS – READ TIMING PARAMETERS

SYMBOL (PCMCIA)	Parameter	150ns		Unit
		Min	Max	
$t_C(R)$	Read Cycle Time	150		ns
$t_A(A)$	Address Access Time		150	ns
$t_A(CE)$	Card Enable Access Time		150	ns
$t_A(OE)$	Output Enable Access Time		75	ns
$t_{SU}(A)$	Address Setup Time		20	ns
$t_{SU}(CE)$	Card Enable Setup Time		0	ns
$t_H(A)$	Address Hold Time		20	ns
$t_H(CE)$	Card Enable Hold Time		20	ns
$t_V(A)$	Output Hold from Address Change		0	ns
$t_{DIS}(CE)$	Output Disable Time from CE#		75	ns
$t_{DIS}(OE)$	Output Disable Time from OE#		75	ns
$t_{EN}(CE)$	Output Enable Time from CE#	5		ns
$t_{EN}(OE)$	Output Enable Time from OE#	5		ns

Note: AC timing diagrams and characteristics are guaranteed to meet or exceed PCMCIA 2.1 specifications.

READ TIMING DIAGRAM



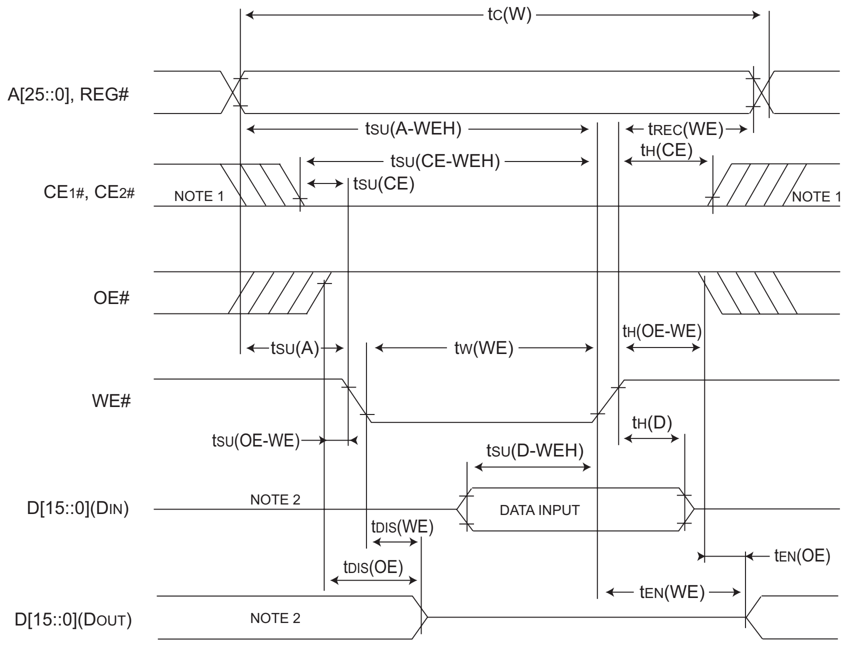
Note: Signal may be high or low in this area.

AC CHARACTERISTICS – WRITE TIMING PARAMETERS

SYMBOL (PCMCIA)	Parameter	150ns		Unit
		Min	Max	
$t_{C}W$	Write Cycle Time	150		ns
t_{W}(WE)	Write Pulse Width	80		ns
t_{SU}(A)	Address Setup Time	20		ns
t_{SU}(A-WEH)	Address Setup Time for WE#	100		ns
t_{SU}(CE-WEH)	Card Enable Setup Time for WE#	100		ns
t_{SU}(D-WEH)	Data Setup Time for WE#	50		ns
t_{H}(D)	Data Hold Time	20		ns
t_{REC}(WE)	Write Recover Time	20		ns
t_{DIS}(WE)	Output Disable Time from WE#		75	ns
t_{DIS}(OE)	Output Disable Time from OE#		75	ns
t_{EN}(WE)	Output Enable Time from WE#	5		ns
t_{EN}(OE)	Output Enable Time from OE#	5		ns
t_{SU}(OE-WE)	Output Enable Setup from WE#	10		ns
t_{H}(OE-WE)	Output Enable Hold from WE#	10		ns
t_{SU}(CE)	Card Enable Setup Time from OE#	0		ns
t_{H}(CE)	Card Enable Hold Time	20		ns

Note: AC timing diagrams and characteristics are guaranteed to meet or exceed PCMCIA 2.1 specifications.

WRITE TIMING DIAGRAM



Notes:
1. Signal may be high or low in this area.
2. When the data I/O pins are in the output state, no signals shall be applied to the data pins (D15 - D0) by the host system.

DATA WRITE AND ERASE PERFORMANCE [1,3]

V_{CC} = 5V ± 5%, 0°C ≤ T_A ≤ + 60°C

SYM	Parameter	Notes	Min	Typ(1)	Max	Units	Test Conditions
t_{WHQV1} t_{EHQV1}	Word/Byte Program time	2,4		8µs	3ms		
t_{WHQV2} t_{EHQV2}	Block Program Time	2		0.5	2.1	sec	Word Program Mode
	Block Erase Time	2		1.1	10	sec	

Notes:
1. Typical: Nominal voltages and T_A = 25°C.
2. Excludes system overhead.
3. Valid for all speed options.
4. To maximize system performance RDY/BSY# signal should be polled.

PRODUCT MARKING

EDI
WED 7P016FLB2600C15 C995 9915

- Company Name — EDI / WED
- Part Number — 7P016FLB2600C15
- Lot Code/Trace Number — C995
- Date Code — 9915

Note:
Some products are currently marked with our pre-merger company name/acronym (EDI). During our transition period, some products will also be marked with our new company name/acronym (WED). Starting October 2000 all PCMCIA products will be marked only with the WED prefix.

PART NUMBERING

7 P 016 FLC26 00 C 15

CARD TECHNOLOGY — 7
- 7 FLASH
- 8 SRAM

PC CARD — P
- P Standard PCMCIA
- R Ruggedized PCMCIA

CARD CAPACITY — 016
- 016 16MB

CARD FAMILY AND VERSION — FLC26
- See Card Family and Version Info. for details (next page)

PACKAGING OPTION — 00
- 00 Standard, type I

TEMPERATURE RANGE — C
- C = Commercial 0°C to +70°C
- I = Industrial -40°C to +85°C

CARD ACCESS TIME — 15
- 15 150ns
- 25 250ns

CARD FAMILY AND VERSION INFORMATION

FLB 21-24	Based on **Am29F016** for 5V only applications
FLB21	No Attribute Memory, no Write Protect
FLB22	With Attribute Memory, no Write Protect
FLB23	No Attribute Memory, with Write Protect
FLB24	With Attribute Memory, with Write Protect

Example P/N **7P XXX FLB 22 SS T ZZ**

FLB 25-28	Based on **Am29F080** for 5V only applications
FLB25	No Attribute Memory, no Write Protect
FLB26	With Attribute Memory, no Write Protect
FLB27	No Attribute Memory, with Write Protect
FLB28	With Attribute Memory, with Write Protect

Example P/N **7P XXX FLB 26 SS T ZZ**

ORDERING INFORMATION

EDI 7P XXX **FLF** YY SS T ZZ

XXX:

002 (1)	2MB
004	4MB
006 (1)	6MB
008	8MB
010 (1)	10MB
012	12MB
014 (1)	14MB
016	16MB
018 (1)	18MB
020	20MB
024 (2)	24MB
028 (2)	28MB
032 (2)	32MB
036 (2)	36MB
040 (2)	40MB

1. available only for FLB26
2. available only for FLB22

FLBYY: Card Version (See Card Family and Version Information)

SS:

00	WEDC Silkscreen
01	Blank Housing, Type I
02	Blank Housing, Type I Recessed

T:

C	Commercial
I**	Industrial

ZZ:

15	150ns

Notes: Options without attribute memory and with hardware write protect switch are available.
** Denotes advanced information.

CIS INFORMATION FOR FLB SERIES CARDS

Address	Value	Description
00H	01H	CISTPL_DEVICE
02H	03H	TPL_LINK
04H	53H	FLASH = 150ns (device writable)
06H	0EH	CARD SIZE: 4MB
	1EH	8MB
	2EH	12MB
	3EH	16MB
	4EH	20MB
	5EH	24MB
	6EH	28MB
	7EH	32MB
	8EH	36MB
	9EH	40MB
08H	FFH	END OF DEVICE
0AH	18H	CISTPL_JEDEC_C
0CH	02H	TPL_LINK
0EH	01H	AMD - ID
10H	ADH	29F016B - ID
12H	17H	CISTPL_DEVICE_A
14H	03H	TPL_LINK
16H	42H	EEPROM - 200ns
18H	01H	Device Size = 2KBytes
1AH	FFH	END OF TUPLE
1CH	1EH	CISTPL_DEVICEGEO
1EH	06H	TPL_LINK
20H	02H	DGTPL_BUS
22H	11H	DGTPL_EBS
24H	01H	DGTPL_RBS
26H	01H	DGTPL_WBS
28H	01H	DGTPL_PART
2AH	01H	FLASH DEVICE
2CH	20H	NON-INTERLEAVED CISTPL_MANFID
2EH	04H	TPL_LINK(04H)
30H	F6H	EDI TPLMID_MANF: LSB
32H	01H	EDI PLMID_MANF: MSB
34H	00H	LSB: Number Not Assign.
36H	00H	MSB: Number Not Assign.
38H	15H	CISTPL_VERS1
3AH	47H	TPL_LINK
3CH	04H	TPLLV1_MAJOR
3EH	01H	TPLLV1_MINOR
40H	45H	E
42H	44H	D
44H	49H	I
46H	37H	7
48H	50H	P
4AH	30H	0
4CH	(1)	x
4EH	(1)	x
50H	46H	F
52H	4CH	L
54H	42H	B
56H	32H	2
58H	(2)	x
5AH	2DH	-
5CH	2DH	-
5EH	2DH	-
60H	31H	1
62H	35H	5
64H	20H	SPACE
66H	00H	END TEXT
68H	43H	C
6AH	4FH	O
6CH	50H	P
6EH	59H	Y
70H	52H	R
72H	49H	I
74H	47H	G
76H	48H	H
78H	54H	T
7AH	20H	SPACE
7CH	45H	E
7EH	4CH	L
80H	45E	E
82H	43H	C
84H	54H	T
86H	52H	R
88H	4FH	O
8AH	4EH	N
8CH	49H	I
8EH	43H	C
90H	20H	SPACE
92H	44H	D
94H	45H	E
96H	53H	S
98H	49H	I
9AH	47H	G
9CH	4EH	N
9EH	53H	S
A0H	20H	SPACE
A2H	49H	I
A4H	4EH	N
A6H	43H	C
A8H	4FH	O
AAH	52H	R
ACH	50H	P
AEH	4FH	O
B0H	52H	R
B2H	41H	A
B4H	54H	T
B6H	45H	E
B8H	44H	D
BAH	20H	SPACE
BCH	00H	END TEXT
BEH	31H	1
C0H	39H	9
C2H	39H	9
C4H	37H	7
C6H	00H	END TEXT
C8H	FFH	END OF LIST

(1)

Address	Value	Description
4CH	30	0
	31	1
	32	2
	33	3
	34	4
4EH	30	0
	32	2
	34	4
	36	6
	38	8

(2)

Address	Value	Description
58H	32	2
	34	4
	36	6
	38	8

Document Title

1 MEGABYTE through 10 MEGABYTE (AMD based)

Revision History

Rev #	History	Release Date	Status
Rev 0	Initial release	12-23-98	
Rev 1	Change logo	5-27-99	
Rev 2	Added page 10	5-31-00	
Rev 3	Corrected timing errors on pages 6 and 7	8-1-00	