Series- 5 FLASH MEMORY CARD

16MB/8MB/4MB/2MB

Product Specification

Documentation History

Version	Description	Date	Written By
1.0	New Issue	Aug. 2006	Greg Liu

Contents

Features

★ PC Card Standard Type 1 form factor

★ Memory Capacity : 2~16 Mega bytes

★ Byte(x8) / word(x16) data bus selectable

★ Optional attribute memory : 8K byte E^2PROM

★ Read voltage : 5V , program/erase voltage : 5V or 12V

★ Fast read access time : 200ns (maximum)

★ Fast byte or word random program : 6us (typ.) @ Vpp = 12V
8us (typ.) @ Vpp = 5V

★ 128K bytes or 64K words per block structure

★ 100000 program/erase cycles per block

★ Fast block erase time : 1 sec (typical) @ Vpp = 12V
1.1 sec (typical) @ Vpp = 5V

★ Automatic erase/write
- command user interface
- status register

★ Enhanced automated suspend capability
- program suspend to read
- block erase suspend to program
- block erase suspend to read

★ Enhanced data protection feature
- flexible block locking

★ Built-in write protect switch

★ Commercial / Industrial grade

General Description

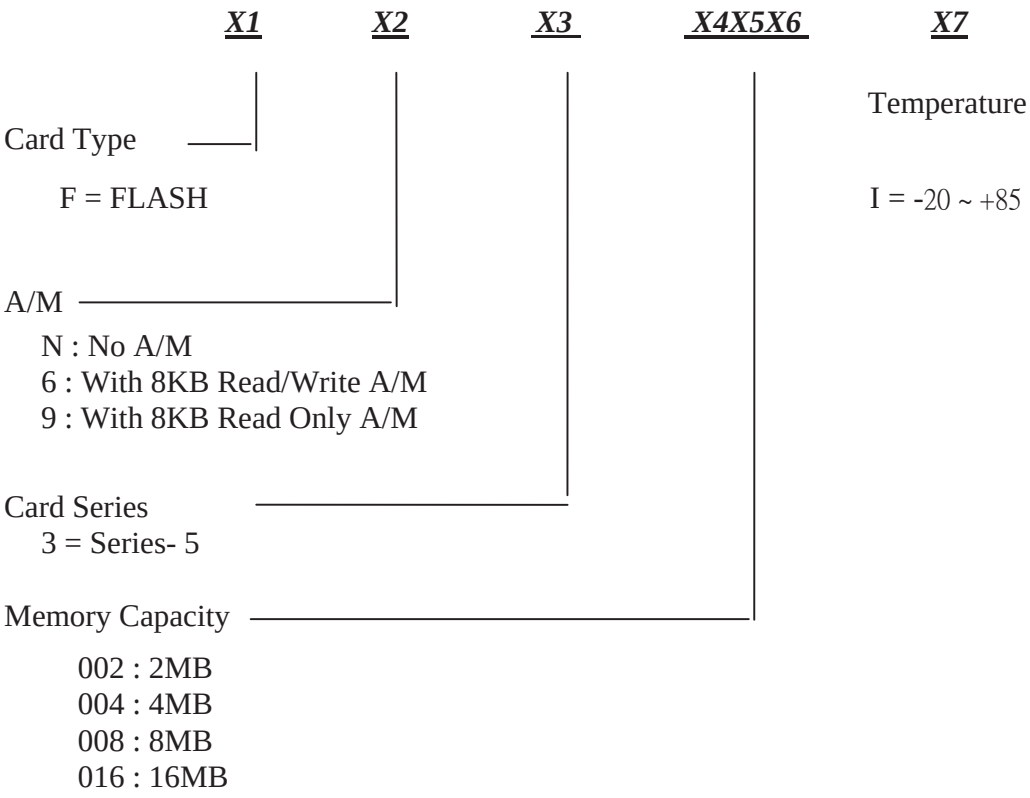
C-ONE's Series- 5 Flash memory cards conform to the PCMCIA / JEIDA international standard and consist of multiple Intel's 28F008S5 (or 28F016S5) or compatible Flash memory devices and decoder IC mounted on a very thin printed circuit board using surface mounting technology.

The Series- 5 Flash memory card family maintains backwards-compatibility with the C-ONE's SERIES 2 Flash memory card family which consist of Intel's 28F008SA Flash memory devices. Key enhancements include : 1) smart voltage allows Vpp to be 5V or 12V, 12V option renders the faster block erase, program performance. 2) enhanced suspend capabilities. 3) in-system block locking.

This series Flash memory cards contain 32 to 512 independent device blocks. Each block can be individually erasable. To support PCMCIA-compatible byte-wide operation , the flash array is divided into 128K bytes per block. To support PCMCIA-compatible word-wide operation , the devices are paired so that each accessible memory block is 64K words.

This series Flash memory cards offer portable , reprogrammable and nonvolatile solid-state storage media and can be used for flexible integration into various system platforms with PCMCIA/JEIDA interface. With the extra and optional 8K bytes "attribute memory" space , the Card Information Structure (CIS) can be written into it by C-ONE or by customer with standard format or customized requirements.

Product Number Definition



Note : A/M means attribute memory.

Product List

Item No.	Part Number	Memory Capacity		Attribute	Memory
		Bytes	Words	Size	Status
1.	FN3002	2M	1M	None	None
2.	FN3004	4M	2M		
3.	FN3008	8M	4M		
4.	FN3016	16M	8M		
5.					
6.					
7.	F63002	2M	1M	8KB E^2PROM	Readable / Writable
8.	F63004	4M	2M		
9.	F63008	8M	4M		
10.	F63016	16M	8M		
11.					
12.					
13.	F93002	2M	1M	8KB E^2PROM	Read only
14.	F93004	4M	2M		
15.	F93008	8M	4M		
16.	F93016	16M	8M		
17.					
18.					

Table 1 ----- with optional 8KB attribute memory

Block Diagram

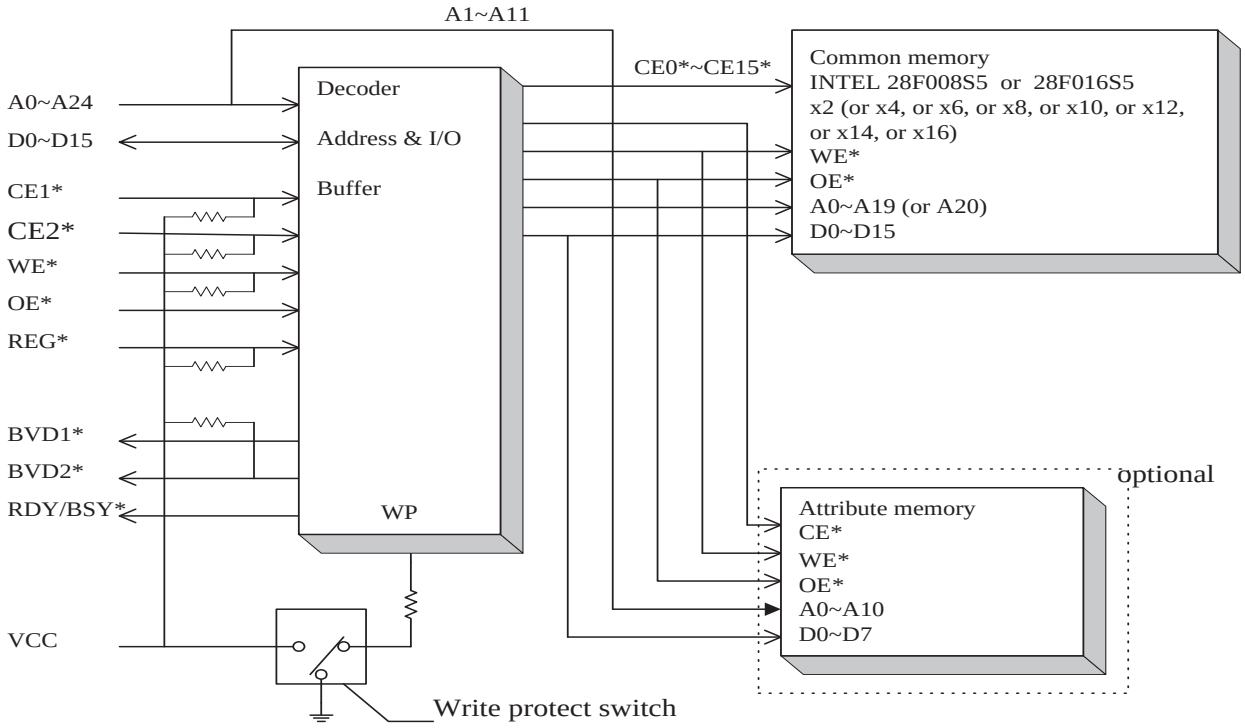


Figure 1 Cards with optional 8KB attribute memory

Pin Configuration (32MB card with attribute memory)

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Pin no.
VCC	RY/BY*	WE*	A14	A13	A8	A9	A11	OE*	A10	CE1*	D7	D6	D5	D4	D3	GND	Pin Name
34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	Pin No.
GND	WP	D2	D1	D0	A0	A1	A2	A3	A4	A5	A6	A7	A12	A15	A16	VPP1	Pin Name
51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	Pin No.
VCC	A21	A20	A19	A18	A17	NC	NC	NC	CE2*	D15	D14	D13	D12	D11	CD1*	GND	Pin Name
68	67	66	65	64	63	62	61	60	59	58	57	56	55	54	53	52	Pin No.
GND	CD2*	D10	D9	D8	BVD1*	BVD2*	REG*	NC	NC	NC	NC	NC	A24	A23	A22	VPP2	Pin Name

Table 3

Note :*mean low active
2MB card series : A21, A22, A23, A24 = NC
4MB card series : A22, A23, A24 = NC
6MB, 8MB card series : A23, A24 = NC
10MB, 12MB, 14MB, 16MB card series : A24 = NC

Pin Description

Symbol	Function	I/O
A0-A24	Addresses	I
D0-D15	Data Inputs/Outputs	I/O
CE1*/CE2*	Card Enable	I
OE*	Output Enable	I
WE*	Write Enable	I
REG*	Attribute Memory Enable	I
WP	Write-protect status Detect	O
BVD1*/BVD2*	Battery Voltage Detect (pull high to Vcc internally)	O
RY/BY*	Ready/Busy status	O
CD1*/CD2*	Card Detect (tied to GND internally)	O
VCC	+5 Volt Power Supply	-
VPP1/VPP2	Write (programming) Power Supply	-
GND	Ground	-
NC	No Connection	-

Table 4

Pin Location

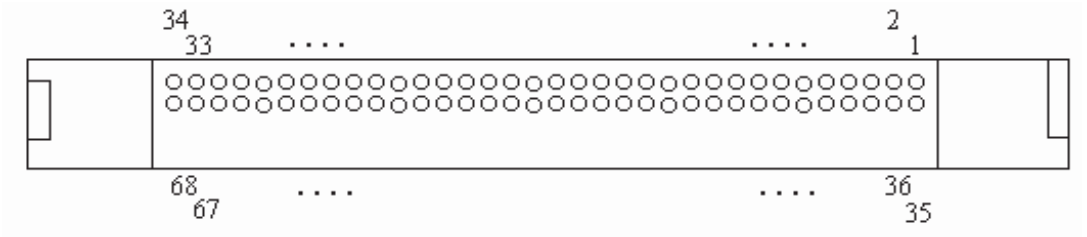


Figure 3 Bottom View (Connector Side)

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit
V_{CC} Supply Voltage	V_{CC}	4.5	5.5	V
V_{PP} Supply Voltage (read)	V_{PPL}	0	6.5	V
V_{PP} Supply Voltage (erase/program)	V_{PPH1}/ V_{PPH2}	4.5/11.4	5.5/12.6	V
Input High Voltage	V_{IH}	2.4	VCC + 0.3	V
Input Low Voltage	V_{IL}	-0.3	0.8	V
Operating Temperature(Commercial)	T_{OPR}	0	70	º C
Operating Temperature(Industrial)	T_{OPR}	-20	85	º C

Table 5

Absolute Maximum Rating *

Parameter	Symbol	Value	Unit
V_{CC} Supply Voltage	V_{CC}	-0.5 to +6.0	V
V_{PP} Supply Voltage (read)	V_{PPL}	-2.0 to +7.0	V
V_{PP} Supply Voltage (erase/write)	V_{PPH}	-2.0 to +14.0	V
Input Voltage	V_{IN}	-0.5 to V_{CC} + 0.3(6V max.)	V
Output Voltage	V_{OUT}	-0.5 to +6.0	V
Operating Temperature (Commercial)	T_{OPR}	0 to +70	º C
Operating Temperature (Industrial)	T_{OPR}	-20 to +85	º C
Storage Temperature	T_{STR}	-40 to +125	º C
Relative Humidity (non-condensing)	H_{UM}	95(maximum)	%

Table 6

***Comments**

Stress above those listed under " Absolute Maximum Ratings " may cause permanent damage to the products. These are stress rating only. Functional operation of these products at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Common Memory Function Table

Function	REG*	CE2*	CE1*	A0	OE*	WE*	V_{PP2}	V_{PP1}	D15-D8	D7-D0
Standby	X	H	H	X	X	X	V_{PPL}	V_{PPL}	High-Z	High-Z
Byte Read	H	H	L	L	L	H	V_{PPL}	V_{PPL}	High-Z	Even Byte Data Out
	H	H	L	H	L	H	V_{PPL}	V_{PPL}	High-Z	Odd Byte Data Out
Word Read	H	L	L	X	L	H	V_{PPL}	V_{PPL}	Odd Byte Data Out	Even Byte Data Out
Odd Byte Only Read	H	L	H	X	L	H	V_{PPL}	V_{PPL}	Odd Byte Data Out	High-Z
Byte Write	H	H	L	L	H	L	V_{PPH}	V_{PPH}	X	Even Byte Data In
	H	H	L	H	H	L	V_{PPH}	V_{PPH}	X	Odd Byte Data In
Word Write	H	L	L	X	H	L	V_{PPH}	V_{PPH}	Odd Byte Data In	Even Byte Data In
Odd Byte Only Write	H	L	H	X	H	L	V_{PPH}	V_{PPH}	Odd Byte Data In	X

Table 7

Attribute Memory Function Table

Function	REG*	CE2*	CE1*	A0	OE*	WE*	V_{PP2}	V_{PP1}	D15-D8	D7-D0
Standby	X	H	H	X	X	X	V_{PPL}	V_{PPL}	High-Z	High-Z
Byte Read	L	H	L	L	L	H	V_{PPL}	V_{PPL}	High-Z	Even Byte Data Out
	L	H	L	H	L	H	V_{PPL}	V_{PPL}	High-Z	Invalid Data Out
Word Read	L	L	L	X	L	H	V_{PPL}	V_{PPL}	Invalid Data Out	Even Byte Data Out
Odd Byte Only Read	L	L	H	X	L	H	V_{PPL}	V_{PPL}	Invalid Data Out	High-Z
Byte Write	L	H	L	L	H	L	V_{PPL}	V_{PPL}	X	Even Byte Data In
	L	H	L	H	H	L	V_{PPL}	V_{PPL}	X	X
Word Write	L	L	L	X	H	L	V_{PPL}	V_{PPL}	X	Even Byte Data In
Odd Byte Only Write	L	L	H	X	H	L	V_{PPL}	V_{PPL}	X	X

Table 8

Notes :

1. L = V_{IL} ; H = V_{IH} ; X = don't care , can be either V_{IH} or V_{IL}.

2. V_{PPH} can be either V_{PPH1} (4.5V to 5.5V) or V_{PPH2} (11.4V to 12.6V).

Card Information Structure

The Card Information Structure (CIS) starts from address zero of the card's Attribute Memory. It contains a variable-length chain of data blocks (tuples). The table shown below is the generic CIS of C-ONE's Series- 5 Flash Memory Card. (For detailed tuple description, please refer to the Metaformat Specification of PC Card Standard.)

Tuple Address (Hex)	Data (Hex)	Description
00	01	CISTPL_DEVICE
02	03	TPL_LINK
04	52	DEVICE_INFO = FLASH 200ns
06	06	CARD SIZE 2MB
	0E	4MB
	16	6MB
	1E	8MB
	26	10MB
	2E	12MB
	36	14MB
	3E	16MB
	4E	20MB
	5E	24MB
	6E	28MB
	7E	32MB
08	FF	CISTPL_END
0A	15	CISTPL_VERS_1
0C	1E	TPL_LINK
0E	04	TPLLV1_MAJOR

Tuple Address (Hex)	Data (Hex)	Description
10	01	TPLLV1_MINOR
12	00	NULL
14	53	S
16	4D	M
18	41	A
1A	52	R
1C	54	T
1E	20	SPACE
20	35	5
22	20	SPACE
24	20	SPACE (for 2/4/6/8MB)
	31	1 (for 10/12/14/16MB)
	32	2 (for 20/24/28MB)
	33	3 (for 32MB)
26	30	0
	32	2
	34	4
	36	6
	38	8

Tuple Address (Hex)	Data (Hex)	Description
28	4D	M
2A	42	B
2C	20	SPACE
2E	46	F
30	4C	L
32	41	A
34	53	S
36	48	H
38	20	SPACE
3A	43	C
3C	41	A
3E	52	R
40	44	D
42	00	Product Information terminated by NULL
44	00	No Additional Product Information
46	00	No Additional Product Information
48	FF	CISTPL_END
4A	18	CISTPL_JEDEC_C
4C	02	TPL_LINK

Tuple Address (Hex)	Data (Hex)	Description
4E	89	INTEL JEDEC ID
50	A6	28F008S5 JEDEC ID
	AA	28F016S5 JEDEC ID
52	1E	CISTPL_DEVICEGEO
54	06	TPL_LINK
56	02	DGTPL_BUS
58	11	DGTPL_EBS
5A	01	DGTPL_RBS
5C	01	DGTPL_WBS
5E	01	DGTPL_PART
60	01	DGTPL_HWIL
62	21	CISTPL_FUNCID
64	02	TPL_LINK
66	01	MEMORY CARD
68	00	NO EXPANSION ROM & POWER ON SELF TEST
6A	FF	CISTPL_END
6C	FF	CISTPL_END

Command Set Table

Command	Bus Cycles Req	First Bus Cycle				Second Bus Cycle				Notes
		Operation	Address	Data		Operation	Address	Data		
				×8 Mode	×16 Mode			×8 Mode	×16 Mode	
Read Array	1	Write	DA	FFH	FFFFH					1
Read Identifier Codes	3	Write	DA	90H	9090H	Read	IA	IID	IID	1,2,3
Read Status Register	2	Write	DA	70H	7070H	Read	DA	SRD	SRD	1,2
Clear Status Register	1	Write	DA	50H	5050H					1
Block Erase	2	Write	BA	20H	2020H	Write	BA	D0H	D0D0H	1
Program	2	Write	WA	40H	4040H	Write	WA	WD	WD	1,2
Program (Alternate)	2	Write	WA	10H	1010H	Write	WA	WD	WD	1,2
Block Erase or Program Suspend	1	Write	DA	B0H	B0B0H					1
Block Erase or Program Resume	1	Write	DA	D0H	D0D0H					1
Set Block Lock-Bit	2	Write	BA	60H	6060H	Write	BA	01H	0101H	1
Clear Block Lock-Bit	2	Write	DA	60H	6060H	Write	DA	D0H	D0D0H	1

Table 9

Notes :

1. DA = A device-level (or device pair) address within the card.

   BA = Address within the block of a specific device (device pair) being erased or locked.

   WA = Address of memory location to be written.

   IA = A device-level identifier address ; 00H for manufacture code (89H). 01H for device code (A6H for 28F008S5, AAH for 28F016S5). xx0002H for block lock configuration. Where xx represents the block number in the device. xx = 00H ~ 0FH for 28F008S5, xx = 00H ~ 1FH for 28F016S5.

2. SRD = Data read from Device Status Register.

   WD = Data to be written at location WA. Data is latched on the rising edge of WE*.

   IID = Data read from identifier codes.

3. Following this command, read operations access manufacturer, device code and block lock configuration.

Command Definitions

When V_{PPL} is applied to the V_{PP1} , V_{PP2} pins , read operations from the Status Register , intelligent identifiers , or array blocks are enabled. Placing V_{PPH1} or V_{PPH2} on V_{PP1} , V_{PP2} pins enables successful block erase, program and lock-bit operations.

Card operations are selected by writing specific commands into the Command User Interface (CUI). Command Set Tables defines this series Flash cards commands.

Read Array Command

Upon initial card powerup and after exit from deep powerdown mode, this series Flash cards default to the Read Array mode. This operation is also entered by writing FFH (or FFFFH) into the Command User Interface (CUI). Microprocessor read cycles retrieve array data. The card remains enabled for reads until the CUI contents are altered by issuing a valid command. Once the internal Write State Machine (WSM) has started a block-erase, program or lock-bit operation, the card will not recognize the Read Array command until the WSM has completed its operation unless the WSM is suspended via an Erase Suspend or Program Suspend command. The Read Array command functions independently of the V_{PP} voltage.

Read Identifier Codes Command

The Read Identifier Codes operation is initiated by writing the Read Identifier Codes command. Following the command write, read cycles from addresses shown in table below access the manufacturer, device and block lock configuration codes. It will remain in this mode until the CUI receives another command.

System software that fully utilizes the PCMCIA specification will not use this mode, as these data are available within the Card Information Structure (CIS). This command functions independently of the V_{PP} voltage.

Code	Byte Access		Word Access		Note
	Address	Data	Address	Data	
Manufacturer ID	000000H	89H	000000H	8989H	
Device ID	000001H	A6H	000002H	A6A6H	28F008S5
	000001H	AAH	000002H	AAAAH	28F016S5
Block Lock Configuration	xx0002H		xx0004H		
Block is unlocked		D0 = ‘0’		D0, D8 = ‘0’	
Block is locked		D0 = ‘1’		D0, D8 = ‘1’	
Reserved		D1 ~ D7		D1~D7,D9~D15	

Note : xx = 00H ~ 0FH (block number) in 28F008S5, xx = 00H ~ 1FH (block number) in 28F016S5.

Read Status Register Command

The 28F008S5 (or 28F016S5) devices on this series card each contains a status register which may be read to determine when a program or block erase operation is complete, and whether that operation completed successfully. The status register may be read at any time by writing the Read Status Register command to the CUI. After writing this command, all subsequent read operations output data from the status register, until the CUI receives another command. The contents of the status register are latched on the falling edge of OE* , CE1* (and/or CE2*) , whichever occurs first. CE1* (and CE2* for odd-byte or word access) or OE* must be toggled to V_{IH} before further reads to update the status register latch. The Read Status Register command functions independently of the V_{PP} voltage.

Clear Status Register Command

Status register bits SR.5, SR.4, SR.3, SR.1 are set to "1"s by the WSM and can only be reset by the Clear Status Register command. These bits indicate various failure conditions (see Table 10 and its description). By allowing system software to control the resetting of these bits, several operations may be performed (such as cumulatively writing several bytes or erasing or locking multiple blocks in sequence). The Status Register may then be polled to determine if an error occurred during that sequence. This adds flexibility to the way the device may be used.

To clear the Status Register, the Clear Status Register command is written to the CUI. The Clear Status Register command functions independently of the V_{PP} voltage. This command is not functional during block erase or program suspend modes.

Block Erase Command

Within a device , erase is performed on one device block at a time , initiated by a two-cycle command sequence. After the system switches V_{PP} to V_{PPH} , an Erase Setup command (20H or 2020H) prepares the CUI for the Erase Confirm command (D0H or D0D0H). The device's WSM controls the erase algorithms internally. After receiving the two-command erase sequence , the device automatically outputs Status Register data when read (See Figure 4). If the command after erase setup is not an Erase Confirm command , the CR sets the Write Failure and Erase Failure bits of the Status Register , places the device into the Read Status Register mode , and waits for another command. The Erase Confirm command enables the WSM for erase (simultaneously closing the address latches for that device's block. The CPU detects the completion of the erase operation by analyzing card-level or device -level indicators. Card-level indicators include the RY/BY* pin and the READY-BUSY* Status Register ; while device-level indicators include the specific device's Status Register. Only the Read Status Register command is valid while the erase operation is active. Upon completion of the erase sequence (see section on Status Register) the device's Status Register reflects the result of the erase operation. The device remains in the Read Status Register mode until the CUI receives a new command.

The two-step block-erase sequence ensures that memory contents are not accidentally erased. Erase attempts while $V_{PPL} < V_{PP} < V_{PPH}$ produce spurious results and are not recommended. Reliable block erasure only occurs when $V_{PP}=V_{PPH}$. In the absence of this voltage , memory contents are protected against erasure. If block erase is attempted while $V_{PP}=V_{PPL}$, the V_{PP} Status bit (SR.3) in the Status Register will be set to "1".

When erase completes , the Erase Status bit (SR.5) in the Status Register should be checked. If an erase error is detected, the device's Status Register should be cleared before system software attempts corrective actions. The CUI remains in Read Status Register mode until receiving a new command.

Note : V_{PPH} can be either V_{PPH1} (4.5V to 5.5V) or V_{PPH2} (11.4V to 12.6V)

Block Erase Suspend/Block Erase Resume Commands

Block Erase Suspend command allows block erase interruption in order to read data from or program data to another block of memory. Once the block erase process starts , writing the Block Erase Suspend command to the CUI requests the WSM to suspend the block erase sequence at a predetermined point in the erase algorithm. The device continues to output Status Register data when read, after the Block Erase Suspend command is written to it.

Polling the device's WSM Status bit (SR.7) and Erase Suspend Status bit (SR.6) in the Status Register, or the card's RY/BY* pin, will determine when the erase operation has been suspended (both bits will be set to '1' and card's RY/BY* pin will also transition to V_{OH}). At this point, a Read Array command can be written to the device's CUI to read data from blocks **other than that which is suspended**. The only other valid commands, at this time, are Read Status Register command and Erase Resume command, at which time the WSM will continue with the block erase process. The WSM Status bit (SR.7) and Erase Suspend Status bit (SR.6) will be cleared to '0' and card's RY/BY* pin will return to V_{OL}. After the Block Erase Resume command is written to CUI, the device automatically outputs Status Register data when read. If V_{PP} goes low during Block Erase Suspend , the V_{PP} Status bit (SR.3) in the Status Regster is set.

Program Command

A data-program operation is executed by a two-command sequence. After the system switches V_{PP} to V_{PPH} , the write setup command (40H or 10H for x8 mode, 4040H or 1010H for x16 mode) is written to the CUI, followed by a second write specifying the address and data (latched on the rising edge of WE*) to be programmed. The device's WSM controls the program and program verify algorithms internally. After receiving the two-command write sequence , the device automatically outputs Status Register data when read. The CPU detects the completion of the program operation by analyzing the WSM Status bit (SR.7) in the Status Register or the output of the RY/BY* pin of the card. Only the Read Status Register command is valid while the program operation is active. Upon completion of the program operation, the Program Status bit (SR.4) should be checked. If error is detected, the status register should be cleared. The WSM verify only detects errors for '1's that do not program to '0's successfully. The CUI remains in the Read Status Register mode until it receives a new command.

Note : V_{PPH} can be either V_{PPH1} (4.5V to 5.5V) or V_{PPH2} (11.4V to 12.6V)

Program Suspend/Program Resume Commands

The Program Suspend command allows program interruption in order to read data from other memory location. Once the program process starts, writing the Program Suspend command to the CUI requests the WSM to suspend the program sequence at a predetermined point in the program algorithm. The device continues to output Status Register data when read, after the Program Suspend command is written to it.

Polling the device's WSM Status bit (SR.7) and Program Suspend Status bit (SR.2) in the Status Register, or the card's RY/BY* pin, will determine when the program operation has been suspended (both bits will be set to '1' and card's RY/BY* pin will also transition to V_{OH}). At this point, a Read Array command can be written to the device's CUI to read data from any memory location **other than the suspended location**. The only other valid commands, at this time, are Read Status Register command and Program Resume command, at which time the WSM will continue with the program process. The WSM Status bit (SR.7) and Program Suspend Status bit (SR.2) will be cleared to '0' and card's RY/BY* pin will return to V_{OL}. After the Program Resume command is written to CUI, the device automatically outputs Status Register data when read. V_{PP} MUST remain at V_{PPH} (the same V_{PP} voltage level used for program operation) during Program Suspend operation.

Note : V_{PPH} can be either V_{PPH1} (4.5V to 5.5V) or V_{PPH2} (11.4V to 12.6V)

Set Block Lock-Bit Command , Clear Block Lock-Bit Command

The Set Block Lock-Bit command enables the host to lock individual blocks in the memory array. The block lock-bits gate the program and block erase operations. All set block lock-bits are cleared in parallel by the Clear Block Lock-Bit command. These are a two-cycle command. The host writes the Set Block Lock-Bit setup command along with the appropriate block or device address followed by the Set Block Lock-Bit confirm command (and the address in the block to be locked). The WSM controls the Set Lock-bit algorithm. The host writes the Clear Block Lock-Bit setup command followed by the Clear Block Lock-Bit confirm command. Upon the completion of the command sequence, the device automatically outputs Status Register data when read. Polling the device's WSM Status bit (SR.7) be set to '1' or the card's RY/BY* pin transition to V_{OH}, the host knows the Set Lock-Bit operation or the Clear Lock-Bit operation completed. The host should check Status Register bit (SR.4) for Set Block Lock-Bit command or Status Register bit (SR.5) for Clear Block Lock-Bit command. If an error is detected, the Status Register should be cleared. The CUI remains in the Read Status Register mode until a new command is issued.

Device Status Register Definition

Each 28F008S5 (or 28F016S5) device in this Series- 5 Flash memory card contains a Status Register which displays the condition of its Write State Machine (WSM). The Status Register is read at any time by writing the Read Status command to the CUI. After writing this command, all subsequent Read operations output data from the Status Register, until another valid command is written to the CUI.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WSMS	ESS	ECLBS	PSLBS	VPPS	PSS	DPS	R

Table 10

Bit 7 (SR.7) --- WSM Status

'1' = Ready '0' = Busy

Before checking Program or Erase Status bit for success, check this bit first for determining the completion of program, block erase , or lock-bit configuration. SR.6 ~ SR.0 are invalid when SR.7 is '0'.

Bit 6 (SR.6) --- Erase Suspend Status

'1' = Block Erase Suspended '0' = Block Erase in Progress/Completed

Bit 5 (SR.5) --- Erase and Clear Block Lock-Bits Status

'1' = Error in Block Erase or Clear Block Lock-Bits operation

'0' = Successful Block Erase or Clear Block Lock-Bits operation

Bit 4 (SR.4) --- Program and Set Block Lock-Bits Status

'1' = Error in Program or Set Block Lock-Bits operation

'0' = Successful Program or Set Block Lock-Bits operation

Bit 3 (SR.3) --- V_{PP} Status

'1' = V_{PP} voltage low detected, operation abort '0' = V_{PP} voltage OK

Bit 2 (SR.2) --- Program Suspend Status

'1' = Program Suspended '0' = Program in Progress/Completed

Bit 1 (SR.1) --- Device Protect Status

'1' = Block Lock-Bit detected, operation abort '0' = Unlock

Bit 0 --- Reserved for future enhancements

This bit is reserved for future use and should be masked out when polling the Status Register.

Device -- Level Automated Program Algorithm

Please refer to the ‘Automated Program Flowchart’ in the INTEL 28F008S5/28F016S5 data sheet.

Device--Level Automated Block Erase Algorithm

Please refer to the ‘Automated Block Erase Flowchart’ in the INTEL 28F008S5/28F016S5 data sheet.

Device--Level Program Suspend/Resume Algorithm

Please refer to the ‘Program Suspend/Resume Flowchart’ in the INTEL 28F008S5/28F016S5 data sheet.

Device--Level Block Erase Suspend/Resume Algorithm

Please refer to the ‘Block Erase Suspend/Resume Flowchart’ in the INTEL 28F008S5/28F016S5 data sheet.

Device--Level Set Block Lock-Bit Algorithm

Please refer to the ‘Set Block Lock-Bit Flowchart’ in the INTEL 28F008S5/28F016S5 data sheet.

Device--Level Clear Block Lock-Bit Algorithm

Please refer to the ‘Clear Block Lock-Bit Flowchart’ in the INTEL 28F008S5/28F016S5 data sheet.

DC Electrical Characteristics

(recommended operating conditions unless otherwise noted)

Symbol	Parameter	8-Bit Mode		16-Bit Mode		Unit	Test Condition
		min	max	min	max		
I_{LI}	Input Leakage Current	-10	10	-10	10	uA	V_{IN} = 0V to V_{CC} (Note 1)
		-70	10	-70	10	uA	V_{IN} = 0V to V_{CC} (Note 2)
I_{LO}	Output Leakage Current	-10	10	-10	10	uA	CE1* = CE2* = V_{IH} or OE* = V_{IH} , V_{OUT} = 0V to V_{CC} (Note 3)
V_{OH}	Output High Voltage	3.8		3.8		V	I_{OH} = -2.0mA (Note 4)
V_{OL}	Output Low Voltage		0.4		0.4	V	I_{OL} = 3.2mA (Note 4)
I_{CCR}	V_{CC} Read Current		60		110	mA	Min. cycle , I_{OUT} = 0mA
I_{CCW}	V_{CC} Program/Set Block Lock-Bit Current		45		80	mA	V_{PP} = V_{PPH1} or V_{PPH2}
I_{CCE}	V_{CC} Block Erase/Clear Block Lock-Bit Current		40		70	mA	V_{PP} = V_{PPH1} or V_{PPH2}
I_{CCWS} I_{CCES}	V_{CC} Program/Block Erase Suspend Current		10		20	mA	Program suspended Block Erase suspended
I_{CCS}	V_{CC} Standby Current		1.5		1.5	mA	CE1* = CE2* = V_{IH} or V_{CC}-0.2V
I_{PPR}	V_{PP} Read Current		0.8		1.0	mA	$V_{PP} > V_{CC}$
I_{PPW}	V_{PP} Program/Set Block Lock-Bit Current		40 15		80 30	mA mA	V_{PP} = 4.5V to 5.5V V_{PP} = 11.4V to 12.6V
I_{PPE}	V_{PP} Block Erase/Clear Block Lock-Bit Current		20 15		40 15	mA mA	V_{PP} = 4.5V to 5.5V V_{PP} = 11.4V to 12.6V
I_{PPWS} I_{PPES}	V_{PP} Program/Block Erase Suspend Current		0.2		0.4	mA	Program/Block Erase Suspended
I_{PPS}	V_{PP} Standby Current		20		40	uA	$V_{PP} \leqq V_{CC}$
V_{PPH1}	V_{PP} Voltage (Program, Block Erase, Set/Clear Block Lock-Bit)	4.5	5.5	4.5	5.5	V	
V_{PPH2}	V_{PP} Voltage (Program, Block Erase, Set/Clear Block Lock-Bit)	11.4	12.6	11.4	12.6	V	

Table 11

Note : 1.) Except CE1* , CE2* , WE* , REG* pins. 2.) For CE1* , CE2* , WE* , REG* pins.
3.) Except BVD1* , BVD2* , CD1* , CD2* pins. 4.) Except CD1* , CD2* pins.

AC Electrical Characteristics

(recommended operating conditions unless otherwise noted)

Read Cycle (Common Memory)

Symbol		Parameter	Note	Min	Max	Unit
t_{AVAV}	t_{RC}	Read Cycle Time		200		ns
t_{AVQV}	t_a (A)	Address Access Time			200	ns
t_{ELQV}	t_a (CE)	Card Enable Access Time			200	ns
t_{GLQV}	t_a (OE)	Output Enable Access Time			100	ns
t_{EHQZ}	t_{dis} (CE)	Output Disable Time (CE*)			90	ns
t_{GHQZ}	t_{dis} (OE)	Output Disable Time (OE*)			90	ns
t_{ELQX}	t_{en} (CE)	Output Enable Time (CE*)		5		ns
t_{GLQX}	t_{en} (OE)	Output Enable Time (OE*)		5		ns
t_{AXQX}	t_v (A)	Data Valid from Address Change		0		ns

Table 12

Write Cycle (Common Memory)

Symbol		Parameter	Min	Typ	Max	Unit
t_{AVAV}	t_{wc}	Write Cycle Time	200			ns
t_{WLWH}	t_w (WE)	Write Pulse Width	100			ns
t_{AVWL}	t_{su} (A)	Address Setup Time	10			ns
t_{AVWH}	t_{su} (A-WEH)	Address Setup Time for WE*	140			ns
t_{VPWH}	t_{vps}	V_{PP} Setup to WE* Going High	100			ns
t_{ELWH}	t_{su} (CE-WEH)	Card Enable Setup Time for WE*	140			ns
t_{DVWH}	t_{su} (D-WEH)	Data Setup Time for WE*	60			ns
t_{WHDX}	t_h (D)	Data Hold Time	30			ns
t_{WHAX}	t_{rec} (WE)	Write Recover Time	30			ns
t_{WHRL}		WE High to RY/BY*			120	ns
t_{WHRH1}		Program Time (5V V_{PP}) Program Time (12V V_{PP})	6.5 4.8	8 6		us us
t_{WHRH2}		Block Erase Time (5V V_{PP}) Block Erase Time (12V V_{PP})	0.9 0.3	1.1 1.0		sec sec
t_{WHRH3}		Set Block Lock-Bit Time (5V V_{PP}) Set Block Lock-Bit Time (12V V_{PP})	9.5 7.8	12 10		us us
t_{WHRH4}		Clear Block Lock-Bit (5V V_{PP}) Clear Block Lock-Bit (12V V_{PP})	0.9 0.3	1.1 1.0		sec sec
t_{WHGL}	t_h (OE-WE)	Write Recovery before Read		10		ns

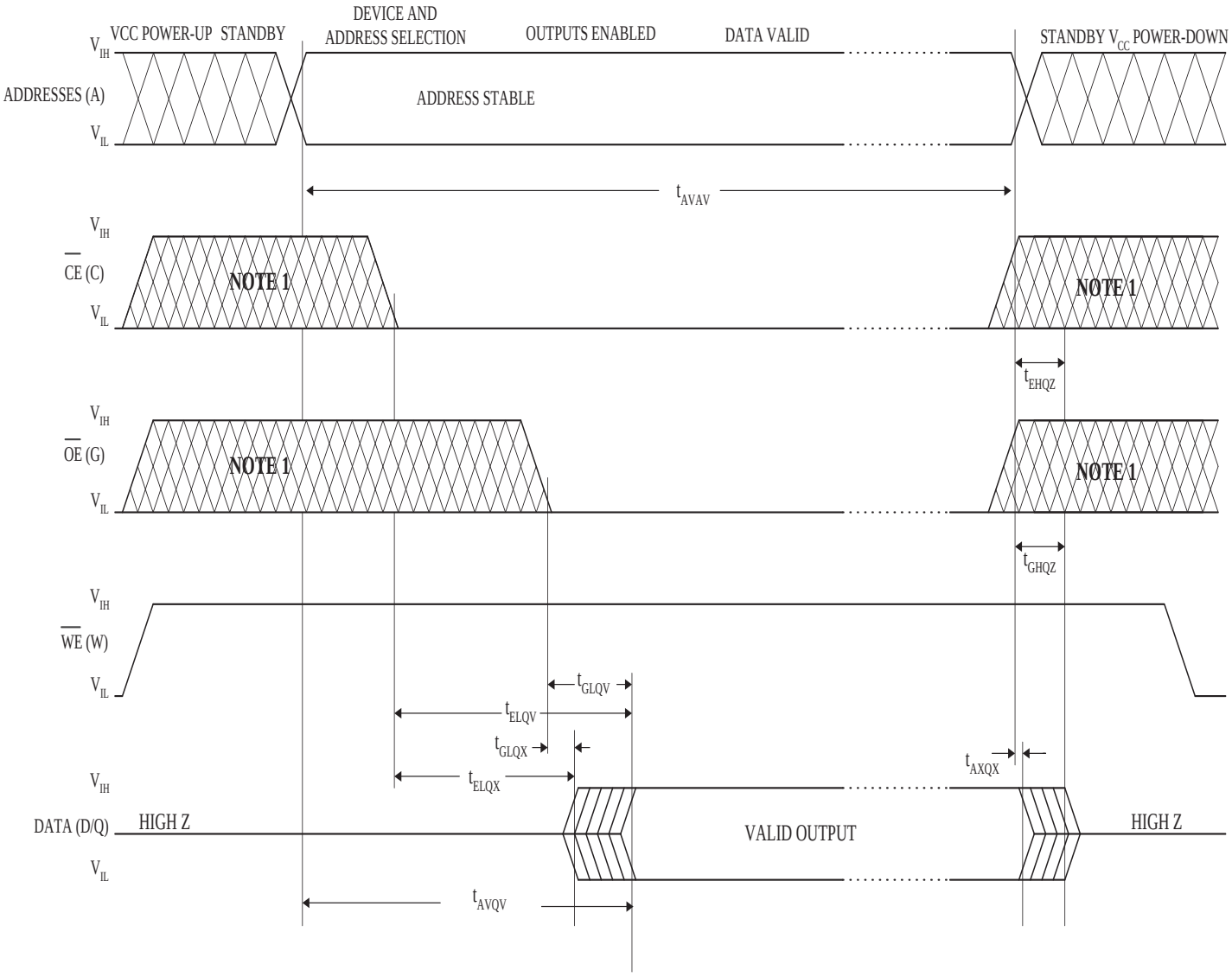
Table 13

Write Cycle (Common Memory) (CE* controlled)

Symbol		Parameter	Min	Typ	Max	Unit
t_{AVAV}	t_{wc}	Write Cycle Time	200	200		ns
t_{ELEH}	t_w (WE)	Card Enable Pulse Width	120	120		ns
t_{AVEL}	t_{su} (A)	Address Setup Time	20	20		ns
t_{AVEH}	t_{su} (A-WEH)	Address Setup Time for CE*	140	140		ns
t_{VPEH}	t_{vps}	VPP Setup to CE* Going High	100	100		ns
t_{WLEH}	t_{su} (CE-WEH)	Write Enable Setup Time for CE*	140	140		ns
t_{DVEH}	t_{su} (D-WEH)	Data Setup Time for CE*	60	60		ns
t_{EHDX}	t_h (D)	Data Hold Time	30	30		ns
t_{EHAX}	t_{rec} (WE)	Write Recover Time	30	30		ns
t_{EHRL}		CE* High to RY/BY*			120	ns
t_{EHRH1}		Program Time (5V V_{PP}) Program Time (12V V_{PP})	6.5 4.8	8 6		us us
t_{EHRH2}		Block Erase Time (5V V_{PP}) Block Erase Time (12V V_{PP})	0.9 0.3	1.1 1.0		sec sec
t_{EHRH3}		Set Block Lock-Bit Time (5V V_{PP}) Set Block Lock-Bit Time (12V V_{PP})	9.5 7.8	12 10		us us
t_{EHRH4}		Clear Block Lock-Bit (5V V_{PP}) Clear Block Lock-Bit (12V V_{PP})	0.9 0.3	1.1 1.0		sec sec
t_{EHGL}	t_h (OE-WE)	Write Recovery before Read	1	10		ns

Table 14

Read Cycle Timing Diagram (Common Memory)



NOTE 1: The hatched area may be either high or low.

Figure 4

Write Cycle Timing Diagram (Common Memory)

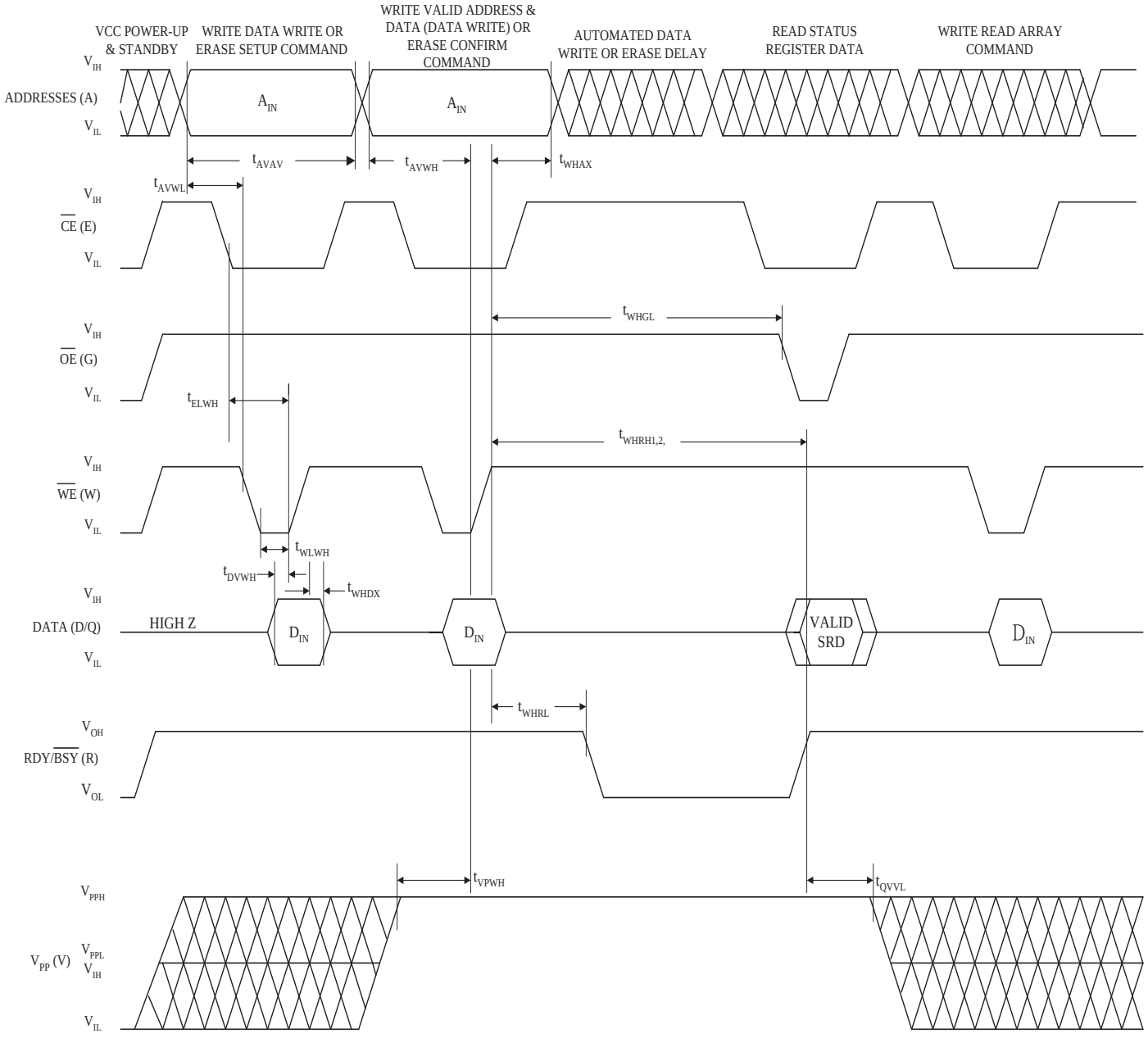


Figure 5

Write Cycle Timing Diagram (Common Memory)

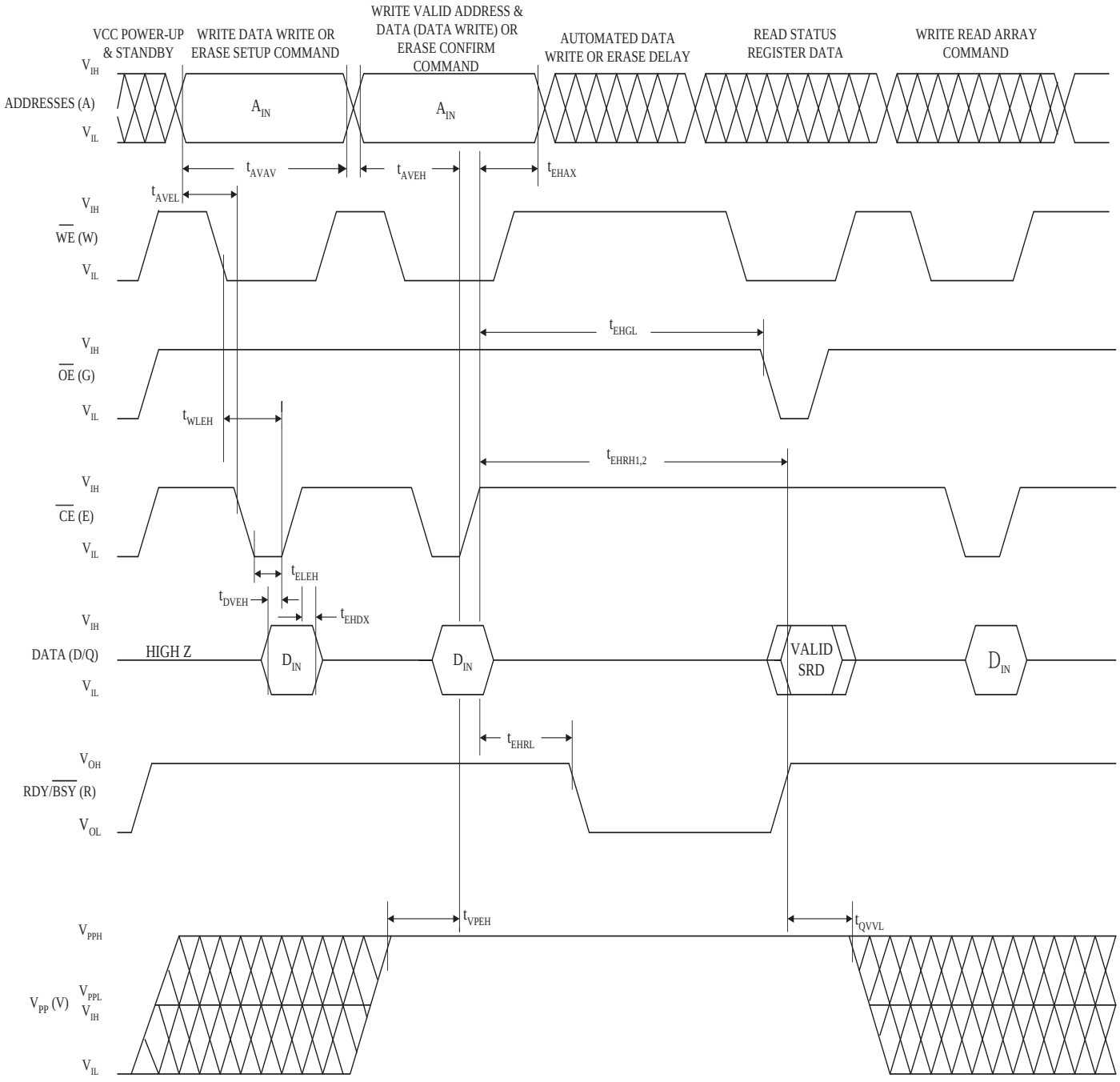


Figure 6

AC Electrical Characteristics (Attribute Memory)

(recommended operating conditions unless otherwise noted)

Read Cycle (Attribute Memory)

Symbol	Parameter	Min.	Max.	Unit	Test Condition
t_{cr}	Read Cycle Time	300		ns	
t_a(A)	Address Access Time		300	ns	
t_a(CE)	Card Select Access Time		300	ns	
t_a(OE)	Output Enable Access Time		150	ns	
t_{dis}(CE)	Output Disable Time (from CE*)		100	ns	
t_{dis}(OE)	Output Disable Time (from OE*)		100	ns	
t_{en}(CE)	Output Enable Time (from CE*)	5		ns	
t_{en}(OE)	Output Enable Time (from OE*)	5		ns	
t_v(A)	Data Hold Time (from address changed)	0		ns	

Table 15

Write Cycle (Attribute Memory)

Symbol	Parameter	Min.	Max.	Unit	Test Condition
t_{cw}	Write Cycle Time		1	ms	
t_{AS}	Address Setup Time	30		ns	
t_{AH}	Address Hold Time	50		ns	
t_{WP}	Write Pulse Width	120		ns	
t_{CS}	Card Enable Time to WE*	15		ns	
t_{CH}	Card Enable Hold Time from WE* High	0		ns	
t_{DS}	Data Setup Time	70		ns	
t_{DH}	Data Hold Time	30		ns	
t_{OES}	OE* Setup Time	30		ns	
t_{OEH}	OE* Hold Time	30		ns	

Table 16

Read Cycle Timing Diagram (Attribute Memory) (REG*=VIL , WE*=VIH)

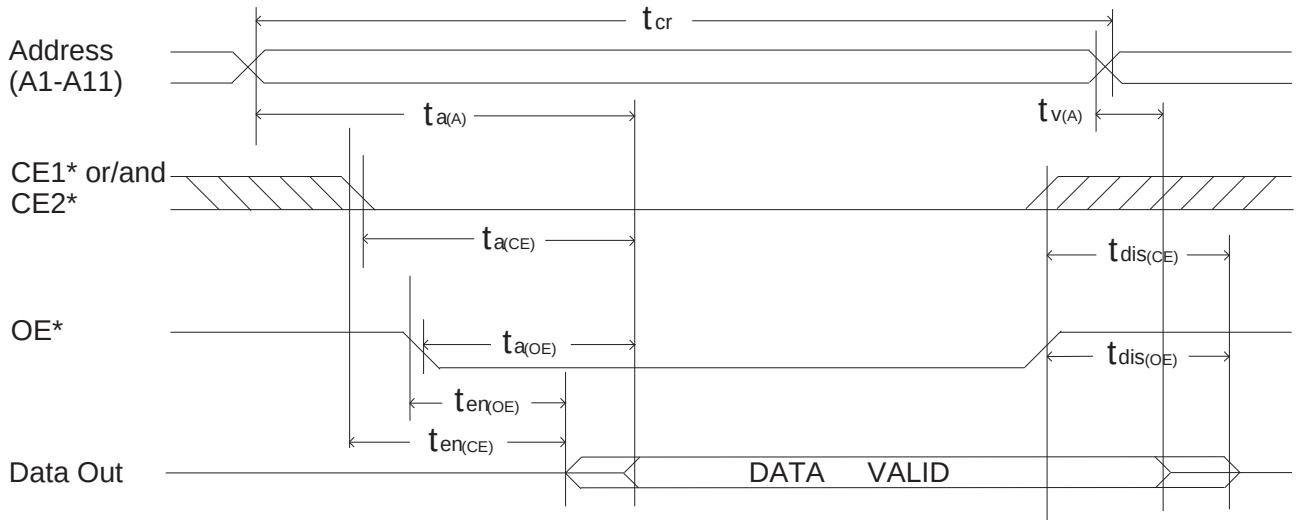


Figure 7

Write Cycle Timing Diagram (Attribute Memory) (REG*=VIL)

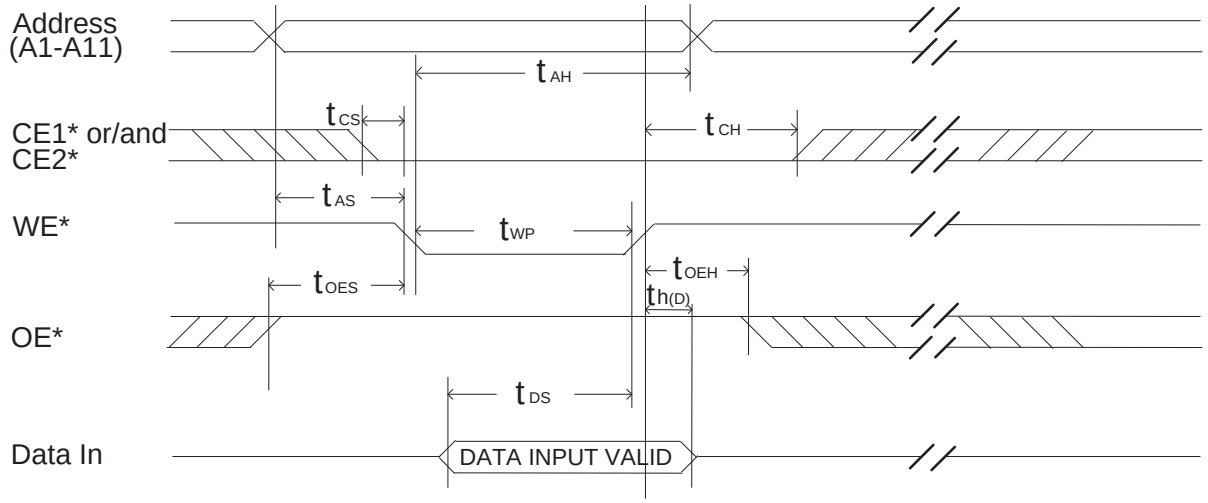
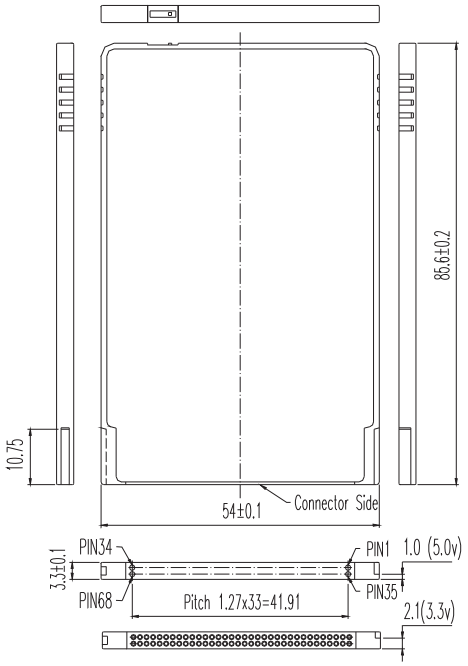
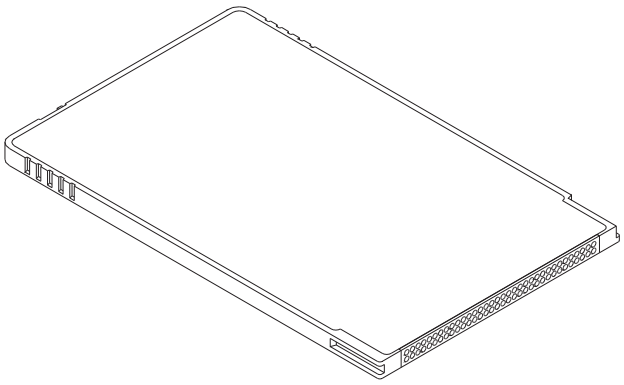


Figure 8

Outline Dimensions (Unit : mm)





FLASH CARD (Write Protect)